

Diagonal 17.5 mm (Type 1.1) CMOS solid-state Image Sensor with Square Pixel for Monochrome Cameras

Description

The IMX541-AAMJ is a diagonal 17.5 mm (Type 1.1) CMOS active pixel type solid-state image sensor with a square pixel array and 20.35 M effective pixels. This chip features a global shutter with variable charge-integration time. This chip operates with analog 3.3 V, 2.9 V, digital 1.1 V, and interface 1.8 V quadruple power supply. High sensitivity and low dark current characteristics are achieved.

(Applications: FA cameras, ITS cameras)

Features

- ◆ CMOS active pixel type dots
- ◆ Built-in timing adjustment circuit, H/V driver and serial communication circuit
- ◆ Global shutter function
- ◆ Input frequency 37.125 MHz / 74.25 MHz / 54 MHz
- ◆ Number of recommended recording pixels: 4504 (H) × 4504 (V) approx. 20.28 M pixels
- ◆ Readout mode
 - All-pixel scan mode
 - Vertical / Horizontal 1/2 Subsampling mode
 - 2 × 2 FD binning mode
 - ROI mode
 - Vertical / Horizontal - Normal / Inverted readout mode
- ◆ Readout rate
 - Maximum frame rate in
 - All-pixel scan mode: 8 bit 42 frame/s, 10 bit 34 frame/s, 12 bit 28 frame/s
- ◆ Pulse Output Function
 - The monitor output for Exposure period
 - Programmable pulse output
- ◆ 8-bit / 10-bit / 12-bit A/D converter
- ◆ CDS / PGA function
 - 0 dB to 24 dB: Analog Gain (0.1 dB step)
 - 24.1 dB to 48 dB: Analog Gain: 24 dB + Digital Gain: 0.1 dB to 24 dB (0.1 dB step)
- ◆ I/O interface
 - SLVS (2 ch / 4 ch / 8 ch switching) output (594 / 297 / 891 / 445.5 Mbps per ch)
 - SLVS - EC (1 Lane / 2 Lane) output (4.752 / 2.376 / 1.188 Gbps per Lane)
- ◆ Recommended lens F number: 2.8 or more (Close side)

Pregius S

* Pregius S is a registered trademark or trademark of Sony Group Corporation or its affiliates. Pregius S is a global shutter sensor technology for active pixel-type CMOS image sensors. By stacking the signal processing on the back illuminated type CMOS Image Sensor it realizes small chip size and high sensitivity, whilst using the high picture quality global shutter pixel technology of Pregius.

Sony reserves the right to change products and specifications without prior notice.

"Sony", "SONY" logo are registered trademarks or trademarks of Sony Group Corporation or its affiliates.

Device Structure

◆ CMOS image sensor			
◆ Image size	Diagonal 17.5 mm (Type 1.1)	Approx. 20.35 M pixels	All-pixel
◆ Total number of pixels	4512 (H) × 4576 (V)	Approx. 20.64 M pixels	
◆ Number of effective pixels	4512 (H) × 4512 (V)	Approx. 20.35 M pixels	
◆ Number of active pixels	4512 (H) × 4512 (V)	Approx. 20.35 M pixels	
◆ Number of recommended recording pixels	4504 (H) × 4504 (V)	Approx. 20.28 M pixels	All-pixel
◆ Unit cell size	2.74 μm (H) × 2.74 μm (V)		
◆ Optical black	Horizontal (H) direction: Front 0 pixel, rear 0 pixel Vertical (V) direction: Front 64 pixels, rear 0 pixel		
◆ Package	230 pin LGA	21.0 mm (H) × 20.0 mm (V)	

Image Sensor Characteristics

(Tj = 60 °C)

Item		Value	Remarks
Sensitivity	Typ.	14510 Digit/lx/s	
Saturation signal	Min.	4094 Digit	

Basic Drive Mode

Drive mode	Recommended number of recording pixels	Maximum frame rate [frame/s]	Output interface	ADC [bit]
All pixel	4504 (H) × 4504 (V) approx. 20.28 M pixels	35	SLVS 8 ch	8
		42	SLVS – EC 2 Lane	
		28	SLVS 8 ch	10
		34	SLVS – EC 2 Lane	
		26	SLVS 8 ch	12
		28	SLVS – EC 2 Lane	
Vertical / Horizontal 1/2 subsampling	2252 (H) × 2252 (V) approx. 5.07 M pixels	119	SLVS 8 ch	8
		157	SLVS – EC 2 Lane	
		96	SLVS 8 ch	10
		127	SLVS – EC 2 Lane	
		95	SLVS 8 ch	12
		109	SLVS – EC 2 Lane	
2 × 2 FD binning mode	2252 (H) × 2252 (V) approx. 5.07 M pixels	119	SLVS 8 ch	8
		157	SLVS – EC 2 Lane	
		96	SLVS 8 ch	10
		127	SLVS – EC 2 Lane	
		95	SLVS 8 ch	12
		109	SLVS – EC 2 Lane	

