Description
The ICX274AQ is a diagonal 8.923mm (Type 1/1.8) interline CCD solid-state image sensor with a square pixel array and 2.01M effective pixels. Progressive scan allows all pixels' signals to be output independently within approximately 1/15 second, and output is also possible using various addition and pulse elimination methods. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. High resolution and high color reproducibility are achieved through the use of R, G, B primary color mosaic filters as the color filters. Further, high sensitivity and low dark current are achieved through the adoption of Super HAD CCD technology.
This chip is suitable for applications such as electronic still cameras, PC input cameras, etc.

Features
• High horizontal and vertical resolution
• Supports the following modes
  - Progressive scan mode (with/without mechanical shutter)
  - 2/8-line readout mode
  - 2/4-line readout mode
  - 2-line addition mode
  - Center scan modes (1), (2) and (3)
  - AF modes (1) and (2)
• Square pixel
• Horizontal drive frequency: 28.6364MHz (typ.), 36.0MHz (max.)
• Reset gate bias are not adjusted
• R, G, B primary color mosaic filters on chip
• High sensitivity, low dark current
• Continuous variable-speed shutter function
• Excellent anti-blooming characteristics
• 20-pin high-precision plastic package

Device Structure
• Interline CCD image sensor
• Image size: Diagonal 8.923mm (Type 1/1.8)
• Total number of pixels: 1688 (H) × 1248 (V) approx. 2.11M pixels
• Number of effective pixels: 1628 (H) × 1236 (V) approx. 2.01M pixels
• Number of active pixels: 1620 (H) × 1220 (V) approx. 1.98M pixels
• Recommended number of recording pixels: 1600 (H) × 1200 (V) approx. 1.92M pixels
• Chip size: 8.50mm (H) × 6.80mm (V)
• Unit cell size: 4.40µm (H) × 4.40µm (V)
• Optical black: Horizontal (H) direction: Front 12 pixels, rear 48 pixels
  - Vertical (V) direction: Front 10 pixels, rear 2 pixels
• Number of dummy bits: Horizontal 28
  - Vertical 1
• Substrate material: Silicon

Wfine CCD
* Wfine CCD is trademark of Sony corporation.
Represents a CCD adopting progressive scan, primary color filter and square pixel.
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Block Diagram and Pin Configuration
(Top View)

Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{\phi}$</td>
<td>Vertical register transfer clock</td>
<td>11</td>
<td>$V_{DD}$</td>
<td>Supply voltage</td>
</tr>
<tr>
<td>2</td>
<td>$V_{\phi3A}$</td>
<td>Vertical register transfer clock</td>
<td>12</td>
<td>$\phi_{RG}$</td>
<td>Reset gate clock</td>
</tr>
<tr>
<td>3</td>
<td>$V_{\phi3B}$</td>
<td>Vertical register transfer clock</td>
<td>13</td>
<td>$H_{\phi2B}$</td>
<td>Horizontal register transfer clock</td>
</tr>
<tr>
<td>4</td>
<td>$V_{\phi3C}$</td>
<td>Vertical register transfer clock</td>
<td>14</td>
<td>$H_{\phi1B}$</td>
<td>Horizontal register transfer clock</td>
</tr>
<tr>
<td>5</td>
<td>$V_{\phi2A}$</td>
<td>Vertical register transfer clock</td>
<td>15</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>6</td>
<td>$V_{\phi2B}$</td>
<td>Vertical register transfer clock</td>
<td>16</td>
<td>$\phi_{SUB}$</td>
<td>Substrate clock</td>
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<td>7</td>
<td>$V_{\phi2C}$</td>
<td>Vertical register transfer clock</td>
<td>17</td>
<td>$C_{SUB}$</td>
<td>Substrate bias**1</td>
</tr>
<tr>
<td>8</td>
<td>$V_{\phi1}$</td>
<td>Vertical register transfer clock</td>
<td>18</td>
<td>$V_{L}$</td>
<td>Protective transistor bias</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>GND</td>
<td>19</td>
<td>$H_{\phi1A}$</td>
<td>Horizontal register transfer clock</td>
</tr>
<tr>
<td>10</td>
<td>$V_{OUT}$</td>
<td>Signal output</td>
<td>20</td>
<td>$H_{\phi2A}$</td>
<td>Horizontal register transfer clock</td>
</tr>
</tbody>
</table>

**1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1µF.
## Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Ratings</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Against $\phi$SUB</td>
<td>$V_{DD}, V_{OUT}, \phi_{RG} - \phi_{SUB} \ (\alpha = A \ to \ C)$</td>
<td>$-40 \ to \ +12$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\phi 2\alpha}, V_{\phi 3\alpha} - \phi_{SUB}$</td>
<td>$-50 \ to \ +15$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\phi 1}, V_{\phi 4}, V_{L} - \phi_{SUB}$</td>
<td>$-50 \ to \ +0.3$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$H_{\phi 1\beta}, H_{\phi 2\beta}, GND - \phi_{SUB} \ (\beta = A, B)$</td>
<td>$-40 \ to \ +0.3$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$CSUB - \phi_{SUB}$</td>
<td>$-25$</td>
<td>to</td>
</tr>
<tr>
<td>Against GND</td>
<td>$V_{DD}, V_{OUT}, \phi_{RG}, CSUB - GND$</td>
<td>$-0.3 \ to \ +22$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\phi 1}, V_{\phi 2\alpha}, V_{\phi 3\alpha}, V_{\phi 4} - GND \ (\alpha = A \ to \ C)$</td>
<td>$-10 \ to \ +18$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$H_{\phi 1\beta}, H_{\phi 2\beta} - GND \ (\beta = A, B)$</td>
<td>$-10 \ to \ +6.5$</td>
<td>V</td>
</tr>
<tr>
<td>Against $V_L$</td>
<td>$V_{\phi 2\alpha}, V_{\phi 3\alpha} - V_L \ (\alpha = A \ to \ C)$</td>
<td>$-0.3 \ to \ +28$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{\phi 1}, V_{\phi 4}, H_{\phi 1\beta}, H_{\phi 2\beta}, GND - V_L \ (\beta = A, B)$</td>
<td>$-0.3 \ to \ +15$</td>
<td>V</td>
</tr>
<tr>
<td>Between input clock pins</td>
<td>Voltage difference between vertical clock input pins</td>
<td>to +15</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$H_{\phi 1\beta} - H_{\phi 2\beta} \ (\beta = A, B)$</td>
<td>$-6.5 \ to \ +6.5$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$H_{\phi 1\beta}, H_{\phi 2\beta} - V_{\phi 4} \ (\beta = A, B)$</td>
<td>$-10 \ to \ +16$</td>
<td>V</td>
</tr>
<tr>
<td>Storage temperature</td>
<td></td>
<td>$-30 \ to \ +80$</td>
<td>°C</td>
</tr>
<tr>
<td>Guaranteed temperature of performance</td>
<td></td>
<td>$-10 \ to \ +60$</td>
<td>°C</td>
</tr>
<tr>
<td>Operating temperature</td>
<td></td>
<td>$-10 \ to \ +75$</td>
<td>°C</td>
</tr>
</tbody>
</table>

*2 $+24$V (Max.) is guaranteed when clock width $< 10$µs, clock duty factor $< 0.1\%$.

$+16$V (Max.) is guaranteed during power-on or power-off.
Bias Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VDD</td>
<td>14.55</td>
<td>15.0</td>
<td>15.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Protective transistor bias</td>
<td>VL</td>
<td>*3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate voltage</td>
<td>VSUB</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>adjustment range</td>
<td>SUB2</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>No line addition*1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>2-line addition*2</td>
<td></td>
<td>8.8</td>
<td>14.4</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Substrate voltage</td>
<td>ΔV SUB</td>
<td>Indicated</td>
<td>Indicated</td>
<td>Indicated</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>adjustment accuracy</td>
<td></td>
<td>voltage – 0.2</td>
<td>voltage + 0.2</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Reset gate clock</td>
<td>φRG</td>
<td>*5</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>

*1 Progressive scan mode, 2/8-line readout mode, 2/4-line readout mode, center scan modes (1) and (3), and AF modes (1) and (2)

*2 2-line addition mode and center scan mode (2)

*3 VL setting is the VVL voltage of the vertical clock waveform, or the same voltage as the VL power supply for the V driver should be used.

*4 Substrate voltage (VSUB) setting value indication
   The substrate voltage (VSUB) for modes without line addition is generated internally.
   The substrate voltage setting value for use with vertical 2-line addition is indicated by a code on the bottom surface of the image sensor. Adjust the substrate voltage to the indicated voltage.

   VSUB2 code – 1-digit indication

   The code and the actual value correspond as follows.

<table>
<thead>
<tr>
<th>VSUB2 code</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
<th>5</th>
<th>6</th>
<th>7</th>
<th>8</th>
<th>9</th>
<th>A</th>
<th>B</th>
<th>C</th>
<th>d</th>
<th>E</th>
<th>f</th>
<th>G</th>
<th>h</th>
</tr>
</thead>
<tbody>
<tr>
<td>Actual value</td>
<td>8.8</td>
<td>9.0</td>
<td>9.2</td>
<td>9.4</td>
<td>9.6</td>
<td>9.8</td>
<td>10.0</td>
<td>10.2</td>
<td>10.4</td>
<td>10.6</td>
<td>10.8</td>
<td>11.0</td>
<td>11.2</td>
<td>11.4</td>
<td>11.6</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

   | VSUB2 code | J | K | L | m | N | P | R | S | U | V | W | X | Y | Z |
   |------------|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
   | Actual value | 11.8 | 12.0 | 12.2 | 12.4 | 12.6 | 12.8 | 13.0 | 13.2 | 13.4 | 13.6 | 13.8 | 14.0 | 14.2 | 14.4 |

   [Example] "h" indicates a VSUB setting of 11.6V.

*5 Do not apply a DC bias to the reset gate clock pin, because a DC bias is generated within the CCD.

DC characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply current</td>
<td>IDD</td>
<td>7.0</td>
<td>10.0</td>
<td>13.0</td>
<td>mA</td>
<td></td>
</tr>
</tbody>
</table>
## Clock Voltage Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Waveform diagram</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Readout clock voltage</strong></td>
<td>$V_{VT}$</td>
<td>14.55</td>
<td>15.0</td>
<td>15.45</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Vertical transfer clock voltage</strong></td>
<td>$V_{VH1}, V_{VH2}$</td>
<td>–0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>2</td>
<td>$V_{VH} = (V_{VH1} + V_{VH2})/2$</td>
</tr>
<tr>
<td></td>
<td>$V_{VH3}, V_{VH4}$</td>
<td>–0.2</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}$</td>
<td>–8.0</td>
<td>–7.5</td>
<td>–7.0</td>
<td>V</td>
<td>2</td>
<td>$V_{VL} = (V_{VL3} + V_{VL4})/2$</td>
</tr>
<tr>
<td></td>
<td>$V_{\phi V}$</td>
<td>6.8</td>
<td>7.5</td>
<td>8.05</td>
<td>V</td>
<td>2</td>
<td>$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 4)</td>
</tr>
<tr>
<td></td>
<td>$V_{VH3} - V_{VH}$</td>
<td>–0.25</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{VH4} - V_{VH}$</td>
<td>–0.25</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{VHH}$</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>2</td>
<td>High-level coupling</td>
</tr>
<tr>
<td></td>
<td>$V_{VHL}$</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>2</td>
<td>High-level coupling</td>
</tr>
<tr>
<td></td>
<td>$V_{VLH}$</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>2</td>
<td>Low-level coupling</td>
</tr>
<tr>
<td></td>
<td>$V_{VLL}$</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>2</td>
<td>Low-level coupling</td>
</tr>
<tr>
<td><strong>Horizontal transfer clock voltage</strong></td>
<td>$V_{\phi H}$</td>
<td>4.75</td>
<td>5.0</td>
<td>5.25</td>
<td>V</td>
<td>3</td>
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</tr>
<tr>
<td></td>
<td>$V_{HL}$</td>
<td>–0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>3</td>
<td></td>
</tr>
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<td></td>
<td>$V_{CR}$</td>
<td>0.8</td>
<td>2.5</td>
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<td>V</td>
<td>3</td>
<td>Cross-point voltage</td>
</tr>
<tr>
<td><strong>Reset gate clock voltage</strong></td>
<td>$V_{\phi G}$</td>
<td>3.0</td>
<td>3.3</td>
<td>5.25</td>
<td>V</td>
<td>4</td>
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<tr>
<td></td>
<td>$V_{RGLH} - V_{RGLL}$</td>
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<td></td>
<td></td>
<td>V</td>
<td>4</td>
<td>Low-level coupling</td>
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<tr>
<td></td>
<td>$V_{RGL} - V_{RGLm}$</td>
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<td></td>
<td></td>
<td>V</td>
<td>4</td>
<td>Low-level coupling</td>
</tr>
<tr>
<td><strong>Substrate clock voltage</strong></td>
<td>$V_{\phi SUB}$</td>
<td>21.5</td>
<td>22.5</td>
<td>23.5</td>
<td>V</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>
Clock Equivalent Circuit Constants

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacitance between vertical transfer clock and GND</td>
<td>$C_{\phi V1}$</td>
<td>3300</td>
<td>pF</td>
<td></td>
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<td></td>
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<tr>
<td></td>
<td>$C_{\phi V2A}, C_{\phi V2B}$</td>
<td>1200</td>
<td>pF</td>
<td></td>
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<tr>
<td></td>
<td>$C_{\phi V2C}$</td>
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<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V3A}, C_{\phi V3B}$</td>
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<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V3C}$</td>
<td>1800</td>
<td>pF</td>
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<td></td>
<td>$C_{\phi V4}$</td>
<td>6800</td>
<td>pF</td>
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<tr>
<td>Capacitance between vertical transfer clocks</td>
<td>$C_{\phi V12 (A, B)}$</td>
<td>120</td>
<td>pF</td>
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<td>$C_{\phi V12C}$</td>
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<td>$C_{\phi V13 (A, B)}$</td>
<td>150</td>
<td>pF</td>
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<td>$C_{\phi V13C}$</td>
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<td>pF</td>
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<td></td>
<td>$C_{\phi V14}$</td>
<td>2700</td>
<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V2 (A, B), 3 (A, B)}$</td>
<td>470</td>
<td>pF</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>$C_{\phi V2 (A, B), 3C}$</td>
<td>680</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{\phi V2 (A, B), 4}$</td>
<td>680</td>
<td>pF</td>
<td></td>
<td></td>
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</tr>
<tr>
<td></td>
<td>$C_{\phi V2C, 3 (A, B)}$</td>
<td>1000</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{\phi V2C, 3C}$</td>
<td>820</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{\phi V2C, 4}$</td>
<td>1800</td>
<td>pF</td>
<td></td>
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<td></td>
</tr>
<tr>
<td></td>
<td>$C_{\phi V3 (A, B), 4}$</td>
<td>820</td>
<td>pF</td>
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<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{\phi V3C, 4}$</td>
<td>1500</td>
<td>pF</td>
<td></td>
<td></td>
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<tr>
<td>Capacitance between horizontal transfer clock and GND</td>
<td>$C_{\phi H1}$</td>
<td>100</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance between horizontal transfer clocks</td>
<td>$C_{\phi H2}$</td>
<td>100</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance between reset gate clock and GND</td>
<td>$C_{\phi RG}$</td>
<td>47</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance between substrate clock and GND</td>
<td>$C_{\phi SUB}$</td>
<td>2</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vertical transfer clock series resistor</td>
<td>$R_{1}, R_{4}$</td>
<td>30</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{2 (A, B, C), 3 (A, B, C)}$</td>
<td>62</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vertical transfer clock ground resistor</td>
<td>$R_{GND}$</td>
<td>15</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Horizontal transfer clock series resistor</td>
<td>$R_{0H}$</td>
<td>7</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Horizontal transfer clock ground resistor</td>
<td>$R_{0H2}$</td>
<td>20</td>
<td>kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reset gate clock and series resistor</td>
<td>$R_{0RG}$</td>
<td>4.7</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1)** Expressions using parentheses such as $C_{\phi V2 (A, B), 3C}$ indicate items which include all combinations of the pins within the parentheses.

For example, $C_{\phi V2 (A, B), 3C}$ indicates [$C_{\phi V2A3C}, C_{\phi V2B3C}$].
Note 2) \( C_{\phi 2 \alpha \beta} \) and \( C_{\phi 3 \alpha \beta} \) (\( \alpha = A \) to \( C \), \( \beta = A \) to \( C \) other than \( \alpha \)) are sufficiently small relative to other capacitance between other vertical clocks in the equivalent circuit, so these are omitted from the equivalent circuit diagram.
Drive Clock Waveform Conditions

(1) Readout clock waveform

\[ V_{\phi} = (V_{\phi 1} + V_{\phi 2})/2 \]
\[ V_{VL} = (V_{VL1} + V_{VL2})/2 \]
\[ V_{\phi} = V_{HH} - V_{HL} (n = 1 \text{ to } 4) \]

(2) Vertical transfer clock waveform

\[ V_{\phi 1} \]
\[ V_{\phi 3A, \phi 3B, \phi 3C} \]
\[ V_{\phi 2A, \phi 2B, \phi 2C} \]
\[ V_{\phi 4} \]
(3) Horizontal transfer clock waveform

Cross-point voltage for the Hφ1β rising side of the horizontal transfer clocks Hφ1β and Hφ2β waveforms is VCR. The overlap period for twh and twl of horizontal transfer clocks Hφ1β and Hφ2β is two. (β = A, B)

(4) Reset gate clock waveform

VRGH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, VRGL is the average value of VRGLH and VRGLL.

\[
VRGL = \frac{VRGLH + VRGLL}{2}
\]

Assuming \( V_{φRG} \) is the minimum value during the interval twh, then:

\[
V_{φRG} = VRGH - VRGL
\]

Negative overshoot level during the falling edge of RG is VRGLm.

(5) Substrate clock waveform

In (Internally generated bias)
### Clock Switching Characteristics (Horizontal drive frequency: 28.6364MHz)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>tw(h)</th>
<th>tw(l)</th>
<th>tr</th>
<th>tf</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout clock</td>
<td>(V_T)</td>
<td>3.3</td>
<td>3.5</td>
<td>0.5</td>
<td>0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vertical transfer clock</td>
<td>(V_{\phi 1}, V_{\phi 4}, V_{\phi 2a}, V_{\phi 3a}) ((\alpha = A \text{ to } C))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>400</td>
</tr>
<tr>
<td>Horizontal transfer clock</td>
<td>(H_{\phi 1} (\beta = A, B))</td>
<td>10</td>
<td>12.5</td>
<td>10</td>
<td>12.5</td>
<td>5</td>
<td>7.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td>12.5</td>
</tr>
<tr>
<td>Reset gate clock</td>
<td>(φ_{RG})</td>
<td>4</td>
<td>7</td>
<td>24</td>
<td>2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Substrate clock</td>
<td>(φ_{SUB})</td>
<td>2.1</td>
<td></td>
<td></td>
<td>0.5</td>
<td>0.5</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>two</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Horizontal transfer clock</td>
<td>(H_{\phi 1A}, H_{\phi 1B}, H_{\phi 2A}, H_{\phi 2B})</td>
<td>8</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

### Clock Switching Characteristics (Horizontal drive frequency: 36MHz)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>tw(h)</th>
<th>tw(l)</th>
<th>tr</th>
<th>tf</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout clock</td>
<td>(V_T)</td>
<td>4.0</td>
<td>4.2</td>
<td>0.5</td>
<td>0.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vertical transfer clock</td>
<td>(V_{\phi 1}, V_{\phi 4}, V_{\phi 2a}, V_{\phi 3a}) ((\alpha = A \text{ to } C))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>15</td>
<td>400</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>8</td>
<td>9</td>
</tr>
<tr>
<td>Reset gate clock</td>
<td>(φ_{RG})</td>
<td>4</td>
<td>5.5</td>
<td>8</td>
<td>2</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td>Substrate clock</td>
<td>(φ_{SUB})</td>
<td>1.67</td>
<td></td>
<td>0.25</td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>two</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Min.</td>
<td>Typ.</td>
<td>Max.</td>
</tr>
<tr>
<td>Horizontal transfer clock</td>
<td>(H_{\phi 1A}, H_{\phi 1B}, H_{\phi 2A}, H_{\phi 2B})</td>
<td>8</td>
<td>9</td>
<td></td>
</tr>
</tbody>
</table>

*1 When two vertical transfer clock drivers CXD3400N are used.

*2 \(tf \geq tr - 2\)ns, and the cross-point voltage (V\(\text{CR}\)) for the \(H_{\phi 1\beta} (\beta = A, B)\) rising side of the \(H_{\phi 1\beta}\) and \(H_{\phi 2\beta}\) waveforms must be \(V\phi H/2\) [V] or more.
Spectral Sensitivity Characteristics (excludes lens characteristics and light source characteristics)
### Image Sensor Characteristics

\((Ta = 25°C)\)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Measurement method</th>
<th>Remarks</th>
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</thead>
<tbody>
<tr>
<td>G Sensitivity</td>
<td>Sg</td>
<td>335</td>
<td>420</td>
<td>545</td>
<td>mV</td>
<td>1</td>
<td>/30s accumulation</td>
</tr>
<tr>
<td>Sensitivity comparison</td>
<td>R</td>
<td>0.35</td>
<td>0.5</td>
<td>0.65</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>B</td>
<td>0.45</td>
<td>0.6</td>
<td>0.75</td>
<td></td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>Saturation signal</td>
<td>Vsat</td>
<td>400</td>
<td></td>
<td></td>
<td>mV</td>
<td>2</td>
<td>Ta = 60°C, No line addition*2</td>
</tr>
<tr>
<td></td>
<td>Vsat2</td>
<td>400</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>2-line addition*3</td>
</tr>
<tr>
<td>Smear</td>
<td>Sm</td>
<td>-100</td>
<td>-92</td>
<td></td>
<td>dB</td>
<td>3</td>
<td>Progressive scan mode*4</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-94</td>
<td>-86</td>
<td></td>
<td></td>
<td></td>
<td>2/4-line readout mode*5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-88</td>
<td>-80</td>
<td></td>
<td></td>
<td></td>
<td>2/8-line readout mode*6</td>
</tr>
<tr>
<td>Video signal shading</td>
<td>SH</td>
<td>20</td>
<td></td>
<td></td>
<td>%</td>
<td>4</td>
<td>Zone 0 and I</td>
</tr>
<tr>
<td></td>
<td></td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Zone 0 to II*</td>
</tr>
<tr>
<td>Uniformity between video signal channels</td>
<td>ΔSrg</td>
<td>8</td>
<td></td>
<td></td>
<td>%</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td></td>
<td>ΔSbg</td>
<td>8</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dark signal</td>
<td>Vdt</td>
<td>8</td>
<td></td>
<td></td>
<td>mV</td>
<td>6</td>
<td>Ta = 60°C, 14.985 frame/s</td>
</tr>
<tr>
<td>Dark signal shading</td>
<td>ΔVdt</td>
<td>2</td>
<td></td>
<td></td>
<td>mV</td>
<td>7</td>
<td>Ta = 60°C, 14.985 frame/s, *7</td>
</tr>
<tr>
<td>Line crawl G</td>
<td>Lcg</td>
<td>3.8</td>
<td></td>
<td></td>
<td>%</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Line crawl R</td>
<td>Lcr</td>
<td>3.8</td>
<td></td>
<td></td>
<td>%</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Line crawl B</td>
<td>Lcb</td>
<td>3.8</td>
<td></td>
<td></td>
<td>%</td>
<td>8</td>
<td></td>
</tr>
<tr>
<td>Lag</td>
<td>Lag</td>
<td>0.5</td>
<td></td>
<td></td>
<td>%</td>
<td>9</td>
<td></td>
</tr>
</tbody>
</table>

*1 Vsat2 is the saturation signal level in 2-line addition mode, and is 200mV per pixel.

*2 Progressive scan mode, 2/8-line readout mode, 2/4-line readout mode, and center scan modes (1) and (3).

*3 2-line addition mode and center scan mode (2).

*4 Same for 2-line addition mode and center scan modes (2) and (3).

*5 Same for center scan mode (1).

*6 Same for AF modes (1) and (2).

*7 Excludes vertical dark signal shading caused by vertical register high-speed transfer.
Zone Definition of Video Signal Shading

Measurement System

Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] and [*C] equals 1.

Image Sensor Characteristics Measurement Method

Color coding of this image sensor & Readout

The primary color filters of this image sensor are arranged in the layout shown in the figure on the left (Bayer arrangement). Gr and Gb denote the G signals on the same line as the R signal and the B signal, respectively.
Readout modes

The diagrams below and on the following pages show the output methods for the following nine readout modes.

<table>
<thead>
<tr>
<th>Progressive scan mode</th>
<th>2/8-line readout mode</th>
<th>2/4-line readout mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 (V2C/V3C)</td>
<td>16 (V2C/V3C)</td>
<td>16 (V2C/V3C)</td>
</tr>
<tr>
<td>15 (V2C/V3C)</td>
<td>15 (V2C/V3C)</td>
<td>15 (V2C/V3C)</td>
</tr>
<tr>
<td>14 (V2A/V3A)</td>
<td>14 (V2A/V3A)</td>
<td>14 (V2A/V3A)</td>
</tr>
<tr>
<td>13 (V2B/V3B)</td>
<td>13 (V2B/V3B)</td>
<td>13 (V2B/V3B)</td>
</tr>
<tr>
<td>12 (V2C/V3C)</td>
<td>12 (V2C/V3C)</td>
<td>12 (V2C/V3C)</td>
</tr>
<tr>
<td>11 (V2C/V3C)</td>
<td>11 (V2C/V3C)</td>
<td>11 (V2C/V3C)</td>
</tr>
<tr>
<td>10 (V2B/V3B)</td>
<td>10 (V2B/V3B)</td>
<td>10 (V2B/V3B)</td>
</tr>
<tr>
<td>9 (V2A/V3A)</td>
<td>9 (V2A/V3A)</td>
<td>9 (V2A/V3A)</td>
</tr>
<tr>
<td>8 (V2C/V3C)</td>
<td>8 (V2C/V3C)</td>
<td>8 (V2C/V3C)</td>
</tr>
<tr>
<td>7 (V2C/V3C)</td>
<td>7 (V2C/V3C)</td>
<td>7 (V2C/V3C)</td>
</tr>
<tr>
<td>6 (V2A/V3A)</td>
<td>6 (V2A/V3A)</td>
<td>6 (V2A/V3A)</td>
</tr>
<tr>
<td>5 (V2B/V3B)</td>
<td>5 (V2B/V3B)</td>
<td>5 (V2B/V3B)</td>
</tr>
<tr>
<td>4 (V2C/V3C)</td>
<td>4 (V2C/V3C)</td>
<td>4 (V2C/V3C)</td>
</tr>
<tr>
<td>3 (V2C/V3C)</td>
<td>3 (V2C/V3C)</td>
<td>3 (V2C/V3C)</td>
</tr>
<tr>
<td>2 (V2B/V3B)</td>
<td>2 (V2B/V3B)</td>
<td>2 (V2B/V3B)</td>
</tr>
<tr>
<td>1 (V2A/V3A)</td>
<td>1 (V2A/V3A)</td>
<td>1 (V2A/V3A)</td>
</tr>
</tbody>
</table>

Note) Blacked out portions in the diagram indicate pixels which are not read out.

Output starts from line 1 in 2/8-line decimation mode.

1. Progressive scan mode
   In this mode, all pixel signals are output in non-interlace format in 1/14.985s. All pixel signals within the same exposure period are read out simultaneously, making this mode suitable for high resolution image capturing.

2. 2/8-line readout mode
   All effective area signals are output in approximately 1/30s by reading out the signals for only two out of eight lines (1st and 6th lines, 9th and 14th lines). This readout mode emphasizes processing speed over vertical resolution, making it suitable for AE/AF and other control and for checking images on LCD viewfinders.

3. 2/4-line readout mode
   All effective area signals are output in approximately 1/20s by reading out the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on).
4. 2-line addition mode

In this mode, the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out, the vertical register is shifted by 2 bits, and then the signals of the remaining two out of the four lines (1st and 2nd lines, 5th and 6th lines, and so on) are read out and added within the vertical register. All effective area signals are output in approximately 1/20s.

5. Center scan mode (1)

In this mode, the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out. The undesired portions are swept by vertical register high-speed transfer, and the vertical 1136-pixel region in the center of the picture is output by the above readout method. The number of output lines is 568 lines at 36MHz, and 434 lines at 28.6364MHz. The frame rate is increased (approximately 30 frames/s) by setting the number of output lines to that of VGA mode, making this mode suitable for VGA moving pictures. (However, the angle of view decreases.)

6. Center scan mode (2)

In this mode, the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out, the vertical register is shifted by 2 bits, and then the signals of the remaining two out of the four lines (1st and 2nd lines, 5th and 6th lines, and so on) are read out and added within the vertical register. The undesired portions are swept by vertical register high-speed transfer, and the vertical 1136-pixel region in the center of the picture is output by the above readout method. The number of output lines is 568 lines at 36MHz, and 434 lines at 28.6364MHz. The frame rate is increased (approximately 30 frames/s) by setting the number of output lines to that of VGA mode, making this mode suitable for VGA moving pictures. (However, the angle of view decreases.)

Note) Blacked out portions in the diagram indicate pixels which are not read out.

After reading out the pixels indicated by ← and transferring two lines, the pixels indicated by ← are read out and two pixels of the same color are added by the vertical transfer block.

<table>
<thead>
<tr>
<th>2-line addition mode</th>
<th>Center scan mode (1)</th>
<th>Center scan mode (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16 (V2C/V3C)</td>
<td>16 (V2C/V3C)</td>
<td>16 (V2C/V3C)</td>
</tr>
<tr>
<td>15 (V2C/V3C)</td>
<td>15 (V2C/V3C)</td>
<td>15 (V2C/V3C)</td>
</tr>
<tr>
<td>14 (V2A/V3A)</td>
<td>14 (V2A/V3A)</td>
<td>14 (V2A/V3A)</td>
</tr>
<tr>
<td>13 (V2B/V3B)</td>
<td>13 (V2B/V3B)</td>
<td>13 (V2B/V3B)</td>
</tr>
<tr>
<td>12 (V2C/V3C)</td>
<td>12 (V2C/V3C)</td>
<td>12 (V2C/V3C)</td>
</tr>
<tr>
<td>11 (V2C/V3C)</td>
<td>11 (V2C/V3C)</td>
<td>11 (V2C/V3C)</td>
</tr>
<tr>
<td>10 (V2B/V3B)</td>
<td>10 (V2B/V3B)</td>
<td>10 (V2B/V3B)</td>
</tr>
<tr>
<td>9 (V2A/V3A)</td>
<td>9 (V2A/V3A)</td>
<td>9 (V2A/V3A)</td>
</tr>
<tr>
<td>8 (V2C/V3C)</td>
<td>8 (V2C/V3C)</td>
<td>8 (V2C/V3C)</td>
</tr>
<tr>
<td>7 (V2C/V3C)</td>
<td>7 (V2C/V3C)</td>
<td>7 (V2C/V3C)</td>
</tr>
<tr>
<td>6 (V2A/V3A)</td>
<td>6 (V2A/V3A)</td>
<td>6 (V2A/V3A)</td>
</tr>
<tr>
<td>5 (V2B/V3B)</td>
<td>5 (V2B/V3B)</td>
<td>5 (V2B/V3B)</td>
</tr>
<tr>
<td>4 (V2C/V3C)</td>
<td>4 (V2C/V3C)</td>
<td>4 (V2C/V3C)</td>
</tr>
<tr>
<td>3 (V2C/V3C)</td>
<td>3 (V2C/V3C)</td>
<td>3 (V2C/V3C)</td>
</tr>
<tr>
<td>2 (V2B/V3B)</td>
<td>2 (V2B/V3B)</td>
<td>2 (V2B/V3B)</td>
</tr>
<tr>
<td>1 (V2A/V3A)</td>
<td>1 (V2A/V3A)</td>
<td>1 (V2A/V3A)</td>
</tr>
</tbody>
</table>

VOUT

Note) Blacked out portions in the diagram indicate pixels which are not read out.

After reading out the pixels indicated by ← and transferring two lines, the pixels indicated by ← are read out and two pixels of the same color are added by the vertical transfer block.
7. Center scan mode (3)
This is the center scan mode using the progressive scan method.
The undesired portions are swept by vertical register high-speed transfer, and the picture center is cut out.
The number of output lines is 580 lines at 36MHz, and 444 lines at 28.6364MHz.

8. AF mode (1)
In this mode, the undesired portions are swept by vertical register high-speed transfer, and the vertical 940-pixel region in the center of the picture is output in approximately 1/60s by reading out the signals for only two out of eight lines (1st and 6th lines, 9th and 14th lines). The number of output lines is 235 lines at 36MHz, and 170 lines at 28.6364MHz. This mode aims for even faster AF control than 2/8-line readout mode.

9. AF mode (2)
In this mode, the undesired portions are swept by vertical register high-speed transfer, and the vertical 300-pixel region in the center of the picture is output in approximately 1/120s by reading out the signals for only two out of eight lines (1st and 6th lines, 9th and 14th lines). The number of output lines is 75 lines at 36MHz, and 43 lines at 28.6364MHz. This mode aims for even faster AF control than 2/8-line readout mode.
Center scan and AF modes

Description of Center Scan and AF Mode Operation

The center scan and AF modes realize high frame rates by sweeping the top and bottom of the picture with high-speed transfer and cutting out the center of the picture. The various readout modes during center scan and AF operation are described below.

- **AF modes**
  - AF mode (1), (2): The output method is the same as readout in 2/8-line readout mode.

- **Center scan modes**
  - Center scan mode (1): The output method is the same as 2/4-line readout mode.
  - Center scan mode (2): The output method consists of 2-line addition readout whereby the signals for only two out of four lines (3rd and 4th lines, 7th and 8th lines, and so on) are read out, the vertical register is shifted by 2 bits, and then the signals of the remaining two out of the four lines (1st and 2nd lines, 5th and 6th lines, and so on) are read out and added within the vertical register.
  - Center scan mode (3): The output method is the same as progressive scan mode.

The readout method, frame rate, number of output lines and other information for each readout mode are shown in the table below.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Readout method</th>
<th>Addition method</th>
<th>Frame rate (frame/s)</th>
<th>Number of output effective pixel data lines</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td>28.6MHz</td>
<td>36MHz</td>
</tr>
<tr>
<td>Progressive scan mode</td>
<td>Progressive scan</td>
<td>None</td>
<td>9.99</td>
<td>14.985</td>
</tr>
<tr>
<td>2/8-line readout mode</td>
<td>2/8-line readout</td>
<td>None</td>
<td>29.97</td>
<td>29.97</td>
</tr>
<tr>
<td>2/4-line readout mode</td>
<td>2/4-line readout</td>
<td>None</td>
<td>19.98</td>
<td>19.98</td>
</tr>
<tr>
<td>2-line addition mode</td>
<td>2/4-line readout</td>
<td>Vertical 2-line</td>
<td>19.98</td>
<td>19.98</td>
</tr>
<tr>
<td>Center scan mode (1)</td>
<td>2/4-line readout</td>
<td>None</td>
<td>29.97</td>
<td>29.97</td>
</tr>
<tr>
<td>Center scan mode (2)</td>
<td>2-line addition readout</td>
<td>Vertical 2-line</td>
<td>29.97</td>
<td>29.97</td>
</tr>
<tr>
<td>Center scan mode (3)</td>
<td>Progressive scan</td>
<td>None</td>
<td>29.97</td>
<td>29.97</td>
</tr>
<tr>
<td>AF mode (1)</td>
<td>2/8-line readout</td>
<td>None</td>
<td>59.94</td>
<td>59.94</td>
</tr>
<tr>
<td>AF mode (2)</td>
<td>2/8-line readout</td>
<td>None</td>
<td>119.88</td>
<td>119.88</td>
</tr>
</tbody>
</table>
Measurement conditions

(1) In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions, and the progressive scan readout mode is used.

(2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the Gr/Gb signal output or the R/B signal output of the measurement system.

Definition of standard imaging conditions

(1) Standard imaging condition I:
Use a pattern box (luminance: 706cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

(2) Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal voltages (VGr, VGb) at the center of each Gr and Gb channel screen, and substitute the values into the following formulas.

\[ V_G = \frac{V_{Gr} + V_{Gb}}{2} \]

\[ S_g = V_G \times \frac{100}{30} \text{ [mV]} \]

2. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 20 times the intensity with the average value of the G channel signal output, 150mV, measure the minimum values of the G, R and B signal outputs.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Gr signal output to 150mV. Measure the average values of the Gr signal output, Gb signal output, R signal output and B signal output (Gra, Gba, Ra, Ba), and then adjust the luminous intensity to 500 times the intensity with the average value of the Gr signal output, 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) independent of the Gr, Gb, R and B signal outputs, and substitute the values into the following formula.

Smear in modes other than progressive scan mode is calculated from the storage time and signal addition method. As a result, 2-line addition mode and center scan modes (2) and (3) are the same as progressive scan mode, 2/4-line readout mode and center scan mode (1) are two times progressive scan mode, and 2/8-line readout mode and AF modes (1) and (2) are four times progressive scan mode.

\[ Sm = 20 \times \log \left( V_{sm} \div \frac{Gra + Gba + Ra + Ba}{4} \times \frac{1}{500} \times \frac{1}{10} \right) \text{ [dB]} \] (1/10V method conversion value)
4. Video signal shading
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the G channel signal output is 150mV. Then measure the maximum value (Gmax [mV]) and minimum value (Gmin [mV]) of the G signal output and substitute the values into the following formula.

\[ SH = \frac{(G_{\text{max}} - G_{\text{min}})}{150} \times 100 \% \]

5. Uniformity between video signal channels
After measuring 4, measure the maximum (Rmax [mV]) and minimum (Rmin [mV]) values of the R signal and the maximum (Bmax [mV]) and minimum (Bmin [mV]) values of the B signal, and substitute the values into the following formulas.

\[ \Delta S_{rg} = \frac{(R_{\text{max}} - R_{\text{min}})}{150} \times 100 \% \]
\[ \Delta S_{bg} = \frac{(B_{\text{max}} - B_{\text{min}})}{150} \times 100 \% \]

6. Dark signal
Measure the average value of the signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
After measuring 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

\[ \Delta V_{dt} = V_{\text{dmax}} - V_{\text{dmin}} \text{ [mV]} \]

8. Line crawl
Set to the standard imaging condition II. Adjusting the luminous intensity so that the value of the Gr signal output is 150mV, and then insert R, G and B filters and measure the difference between G signal lines (\(\Delta G_{\text{lr}}, \Delta G_{\text{lg}}, \Delta G_{\text{lb}} \text{ [mV]}\)) as well as the value of the G signal output (Gar, Gag, Gab). Substitute the values into the following formula.

\[ L_{ci} = \frac{\Delta G_{\text{li}}}{G_{\text{ai}}} \times 100 \% \text{ (i = r, g, b)} \]

9. Lag
Adjust the Y signal output generated by the strobe light to 150mV. After setting the strobe light so that it strobos with the following timing, measure the residual signal amount (Vlag). Substitute the value into the following formula.

\[ \text{Lag} = \left( \frac{V_{\text{lag}}}{150} \right) \times 100 \% \]

---

**Diagram for Lag**

- **Strobe light timing**
  - Light
- **Output**
  - Y signal output 150mV
  - Vlag (lag)

---

- **VD**
  - Strobe light timing
  - Light
  - Y signal output 150mV
  - Vlag (lag)
**Note)** Substrate bias control
Switch the substrate bias adjustment input voltage to DCIN before adjusting the substrate bias in 2-line addition mode and center scan mode (2).
Drive Timing Chart (Vertical Sync)  Progressive Scan Mode

Note) The 1252H horizontal period at 36MHz is 480clk; the 1493H horizontal period at 28MHz is 1860clk.
Drive Timing Chart (Vertical Sync)  Progressive Scan Mode

"a" enlarged

H1A/H1B

V1

V2A/V2B/V2C

V3A/V3B/V3C

V4

18 18 18 18 18 18 18 18 60

1100 1250
Drive Timing Chart (Vertical Sync)  Progressive Scan Mode (With Mechanical Shutter)

Note) The 1564 and 1565H horizontal periods at 36MHz are 1021clk; the 1742H horizontal period at 28MHz is 1530clk.
Drive Timing Chart (Vertical Sync)

Progressive Scan Mode (With Mechanical Shutter)

"b" enlarged

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

13440 bits
Note) The 511H horizontal period at 36MHz is 1680clk; the 406 and 407H horizontal periods at 28MHz are 1470clk.
Drive Timing Chart (Vertical Sync) 2/8-line Readout Mode

"a" enlarged

H1A/H1B

V1

V2A

V2B/V2C

V3A

V3B/V3C

V4

18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18

18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 42

1100 1250

18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 60

18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18
Note) The 871H horizontal period at 36MHz is 900clk; the 693H horizontal period at 28MHz is 810clk.
"a" enlarged

Drive Timing Chart (Vertical Sync)  2/4-line Readout Mode

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

18 54 18 18 18 18 18 18 18 18 18 18 18 18 18 18 54 150 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 66

600 750

18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 54 150 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 66
Note) The 871H horizontal period at 36MHz is 900clk; the 693H horizontal period at 28MHz is 810clk.
Drive Timing Chart (Vertical Sync) 2-line Addition Mode

"a" enlarged

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

600 750
Note) The 462H horizontal period is 1230clk.
Drive Timing Chart (Vertical Sync)  Center Scan Mode (1)/(36MHz)

Note) The 581H horizontal period is 601clk.
Drive Timing Chart (Vertical Sync)  
Center Scan Mode (1)  

"a" enlarged
"b" enlarged

Drive Timing Chart (Vertical Sync)  Center Scan Mode (1)/(28.6MHz)

28980 bits = 14H

27936 bits
Drive Timing Chart (Vertical Sync)  Center Scan Mode (1)/(36MHz)

"b" enlarged
Note) The 462H horizontal period is 1230clk.
Drive Timing Chart (Vertical Sync)  Center Scan Mode (2)/(36MHz)

Note) The 581H horizontal period is 601clk.
### Drive Timing Chart (Vertical Sync)  
**Center Scan Mode (2)**

"a" enlarged

<table>
<thead>
<tr>
<th>Timing Event</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>H1A/H1B</td>
<td></td>
</tr>
<tr>
<td>V1</td>
<td></td>
</tr>
<tr>
<td>V2C</td>
<td></td>
</tr>
<tr>
<td>V2A/V2B</td>
<td></td>
</tr>
<tr>
<td>V3C</td>
<td></td>
</tr>
<tr>
<td>V3A/V3B</td>
<td></td>
</tr>
<tr>
<td>V4</td>
<td></td>
</tr>
</tbody>
</table>

- 600  
- 750  

- 54  
- 150  

![Drive Timing Chart](image-url)
Drive Timing Chart (Vertical Sync)  Center Scan Mode (2)/(28.6MHz)

"b" enlarged

H1A/H1B  V1  V2C  V2A/V2B  V3C  V3A/V3B  V4

# (3 + 5)  # (4 + 6)  # (185 + 187)

28980 bits = 14H

27936 bits
"b" enlarged

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

18 18 18 18 18 18 18 18
# (3 + 5) # (4 + 6) # (50 + 52)

10350 bits = 5H

8784 bits
Drive Timing Chart (Vertical Sync)  Center Scan Modes (1) and (2)/(28.6MHz)

"d" enlarged

16560 bits

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4
Drive Timing Chart (Vertical Sync)  Center Scan Modes (1) and (2)/(36MHz)

"d" enlarged

H1A/H1B

V1
V2C
V2A/V2B
V3C
V3A/V3B
V4

6210 bits

#1 #2 #3 #63
Drive Timing Chart (Vertical Sync)  Center Scan Mode (3)/(28.6MHz)

Note) The 498H horizontal period is 1260clk.
Note) The 626H horizontal period is 1200clk.
Drive Timing Chart (Vertical Sync)  Center Scan Mode (3)/(28.6MHz)

"b" enlarged

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

59520 bits = 31H

58608 bits
Drive Timing Chart (Vertical Sync)  Center Scan Mode (3)/(36MHz)

"b" enlarged

49920 bits = 26H

48816 bits
Drive Timing Chart (Vertical Sync) Center Scan Mode (3)/(28.6MHz)

"d" enlarged

H1A/H1B  V1  V2C  V2A/V2B  V3C  V3A/V3B  V4
Drive Timing Chart (Vertical Sync)  Center Scan Mode (3)/(36MHz)

"d" enlarged

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

#1  #2  #3  #330

28800 bits
Note) The 203 and 204H horizontal periods are 1323clk.
Note) The 256H horizontal period is 840clk.
"b" enlarged

Drive Timing Chart (Vertical Sync)  AF Mode (1)/(28.6MHz)

H1A/H1B
V1
V2C
V2A/V2B
V3C
V3A/V3B
V4

42336 bits = 18H
41904 bits =
"b" enlarged

Drive Timing Chart (Vertical Sync)  AF Mode (1)/(36MHz)

- H1A/H1B
- V1
- V2C
- V2A/V2B
- V3C
- V3A/V3B
- V4

23520 bits = 10H

22896 bits
Drive Timing Chart (Vertical Sync)  AF Mode (1)/(28.6MHz)

"d" enlarged

H1A/H1B
V1
V2C
V2A/V2B
V3C
V3A/V3B
V4

25872 bits
Drive Timing Chart (Vertical Sync)  AF Mode (1)/(36MHz)

"d" enlarged

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

14112 bits
Drive Timing Chart (Vertical Sync)  AF Mode (2)/(28.6MHz)

Note) The 102H horizontal period is 1323clk.
Note) The 128H horizontal period is 1596clk.
Drive Timing Chart (Vertical Sync)  
AF Mode (2)/(28.6MHz)

"b" enlarged

H1A/H1B  H2C  V2A/V2B  V2C  V3A/V3B  V3C  V4

79956 bits = 34H

79968 bits
Drive Timing Chart (Vertical Sync)  AF Mode (2)/(28.6MHz) 

"d" enlarged

H1A/H1B

V1

V2C

V2A/V2B

V3C

V3A/V3B

V4

47040 bits

47040 bits
Drive Timing Chart (Vertical Sync)  AF Mode (2)/(36MHz)

"d" enlarged

H1A/H1B
V1
V2C
V2A/V2B
V3C
V3A/V3B
V4

42336 bits

1  #1  #2  #3  #564
Drive Timing Chart (Horizontal Sync)  
AF Modes (1) and (2)
Drive Timing Chart (Vertical Sync)  AF Modes (1) and (2)

"a" enlarged

H1A/H1B

V1

V2A

V2B/V2C

V3A

V3B/V3C

V4
Notes of Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   a) Either handle bare handed or use non-chargeable gloves, clothes or material.
      Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensors.
   e) For the shipment of mounted substrates, use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a ground 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
   c) To dismount an image sensor, do not use a solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3) Dust and dirt protection
Image sensors are packed and delivered by taking care of protecting its glass plates from harmful dust and dirt. Clean glass plates with the following operations as required, and use them.
   a) Perform all assembly operations in a clean room (class 1000 or less).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface, blow it off with an air blower. (For dirt stuck through static electricity ionized air is recommended.)
   c) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   d) Keep in a case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Installing (attaching)
   a) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)

   ![Diagram](image_url)

   b) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
c) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to other locations as a precaution.
d) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.
e) If the leads are bent repeatedly and metal, etc., clash or rub against the package, the dust may be generated by the fragments of resin.
f) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

5) Others
a) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminous objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloring of the color filter will possibly be accelerated. In such a case, it is advisable that taking-lens with the automatic-iris and closing of the shutter during the power-off mode should be properly arranged. For continuous using under cruel condition exceeding the normal using condition, consult our company.
b) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.
c) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.
d) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.

The cross section of lead frame can be seen on the side of the package for structure A.
1. “A” is the center of the effective image area.

2. The two points “B” of the package are the horizontal reference. 
   The point “B’” of the package is the vertical reference.

3. The bottom “C” of the package, and the top of the cover glass “D” are the height reference.

4. The center of the effective image area relative to “B” and “B’” is (H, V) = (6.9, 6.0) ± 0.075mm.

5. The rotation angle of the effective image area relative to H and V is ± 1˚.

6. The height from the bottom “C” to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass “D” to the effective image area is 1.49 ± 0.15mm.

7. The tilt of the effective image area relative to the bottom “C” is less than 50μm.
   The tilt of the effective image area relative to the top “D” of the cover glass is less than 50μm.

8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.

9. The notches on the bottom of the package are used only for directional index, they must not be used for reference of fixing.