Diagonal 6.0mm (Type 1/3) Progressive Scan CCD Image Sensor for B/W Cameras

ICX445ALA

Description

The ICX445ALA is a diagonal 6.0mm (Type 1/3) interline CCD solid-state image sensor with a square pixel array and 1.25M effective pixels. Progressive scan enables all pixel signals to be output separately and sequentially within 1/22.5 second. The sensitivity and smear are improved drastically through the adoption of EXview HAD CCD technology.

Features

- Supports following readout modes
  - All-pixel scan mode (15 frame/s, 12.5 frame/s, 22.5 frame/s: Max.)
  - Center cut-out mode (30 frame/s, 25 frame/s)
- Horizontal drive frequency: 36.0MHz, 29.0MHz
- High resolution, high sensitivity, low dark current, low smear
- Excellent anti-blooming characteristics
- No voltage adjustments (Reset gate and substrate bias need no adjustment.)
- 24-pin high precision plastic package (Dual-surface reference available)

Package

24-pin DIP (Plastic)

EXview HAD CCD™

* EXview HAD CCD is a trademark of Sony Corporation. The EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation Diode) sensor.

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Device Structure

- Interline CCD image sensor
- Image size
  Diagonal 6.0mm (Type 1/3)
- Total number of pixels
  1348 (H) × 976 (V) approx. 1.32M pixels
- Number of effective pixels
  1296 (H) × 966 (V) approx. 1.25M pixels
- Number of active pixels
  1280 (H) × 960 (V) approx. 1.23M pixels
- Chip size
  6.26mm (H) × 5.01mm (V)
- Unit cell size
  3.75μm (H) × 3.75μm (V)
- Optical black
  Horizontal (H) direction: front 12 pixels, rear 40 pixels
  Vertical (V) direction: front 8 pixels, rear 2 pixels
- Number of dummy bits
  Horizontal (H) direction: front 4 pixels
  Vertical (V) direction: front 2 pixels
- Substrate material
  Silicon

Optical Black Position

(Top View)
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Block Diagram and Pin Configuration

Pin Description

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Vφ2B</td>
<td>Vertical register transfer clock</td>
<td>13</td>
<td>VOUT</td>
<td>Signal output</td>
</tr>
<tr>
<td>2</td>
<td>Vφ2A</td>
<td>Vertical register transfer clock</td>
<td>14</td>
<td>GND</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>Vφ3B</td>
<td>Vertical register transfer clock</td>
<td>15</td>
<td>GND</td>
<td>GND</td>
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<tr>
<td>4</td>
<td>Vφ3A</td>
<td>Vertical register transfer clock</td>
<td>16</td>
<td>φRG</td>
<td>Reset gate clock</td>
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<tr>
<td>5</td>
<td>Vφ1B</td>
<td>Vertical register transfer clock</td>
<td>17</td>
<td>LHφ1</td>
<td>Horizontal register final stage transfer clock</td>
</tr>
<tr>
<td>6</td>
<td>Vφ1A</td>
<td>Vertical register transfer clock</td>
<td>18</td>
<td>Hφ2A</td>
<td>Horizontal register transfer clock</td>
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<tr>
<td>7</td>
<td>Vφ4B</td>
<td>Vertical register transfer clock</td>
<td>19</td>
<td>Hφ1A</td>
<td>Horizontal register transfer clock</td>
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<tr>
<td>8</td>
<td>Vφ4A</td>
<td>Vertical register transfer clock</td>
<td>20</td>
<td>Hφ1B</td>
<td>Horizontal register transfer clock</td>
</tr>
<tr>
<td>9</td>
<td>VφST</td>
<td>Horizontal addition control clock</td>
<td>21</td>
<td>Hφ2B</td>
<td>Horizontal register transfer clock</td>
</tr>
<tr>
<td>10</td>
<td>VφHL</td>
<td>Horizontal addition control clock</td>
<td>22</td>
<td>φSUB</td>
<td>Substrate clock</td>
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<tr>
<td>11</td>
<td>VL</td>
<td>Protective transistor bias</td>
<td>23</td>
<td>NC</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>NC</td>
<td></td>
<td>24</td>
<td>VDD</td>
<td>Supply voltage</td>
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</table>
### Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Against φSUB</td>
<td>VDD, VOUT, φRG – φSUB</td>
<td>–39 to +12</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vφ1A, Vφ1B, Vφ4A, Vφ4B, VφST, VφHLD, VL – φSUB</td>
<td>–46 to +0.3</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hφ1A, Hφ1B, Hφ2A, Hφ2B, LHφ1, GND – φSUB</td>
<td>–39 to +0.3</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Against GND</td>
<td>VDD, VOUT, φRG – GND</td>
<td>–0.3 to +20</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hφ1A, Hφ1B, Hφ2A, Hφ2B, LHφ1 – GND</td>
<td>–9.0 to +4.2</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Against VL</td>
<td>Vφ2A, Vφ2B, Vφ3A, Vφ3B – VL</td>
<td>–0.3 to +25</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vφ1A, Vφ1B, Vφ4A, Vφ4B, VφST, VφHLD, Hφ1A, Hφ1B, Hφ2A, Hφ2B, LHφ1, GND – VL</td>
<td>–0.3 to +13</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Between input clock pins</td>
<td>Potential difference between vertical clock input pins</td>
<td>to +13</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hφ1A, Hφ1B – Hφ2A, Hφ2B</td>
<td>–5 to +5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Hφ1A, Hφ1B, Hφ2A, Hφ2B – Vφ4B, VφHLD</td>
<td>–13 to +13</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Storage temperature</td>
<td></td>
<td>–30 to +80</td>
<td>°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating temperature</td>
<td></td>
<td>–10 to +60</td>
<td>°C</td>
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</table>

*1 Guaranteed up to 25V when the clock width < 10μs and the clock duty factor < 0.1%.

### Bias Conditions

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VDD</td>
<td>14.55</td>
<td>15.0</td>
<td>15.45</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Protective transistor bias</td>
<td>VL</td>
<td>*1</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Substrate clock</td>
<td>φSUB</td>
<td>*2</td>
<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>Reset gate clock</td>
<td>φRG</td>
<td>*2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*1 For the VL setting, use the VVL voltage of the vertical clock waveform or the same voltage as the VL power supply of the V driver.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated internally.

### DC Characteristics

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
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<tr>
<td>Supply current</td>
<td>IODD</td>
<td>10.0</td>
<td>mA</td>
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</table>
## Clock Voltage Conditions

<table>
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<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Waveform diagram</th>
<th>Remarks</th>
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<tbody>
<tr>
<td><strong>Readout clock voltage</strong></td>
<td>VVT</td>
<td>14.55</td>
<td>15.0</td>
<td>15.45</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>VVH2, VVH3</td>
<td>–0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>2</td>
<td>VVH = (VVH2 + VVH3)/2</td>
</tr>
<tr>
<td></td>
<td>VVH1, VVH4, VVHSTR, VVHLD</td>
<td>–0.2</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VVL1, VVL2, VVL3, VVL4, VVLSTR, VVLHLD</td>
<td>–8.8</td>
<td>–8.5</td>
<td>–8.2</td>
<td>V</td>
<td>2</td>
<td>VVL = (VVL1 + VVL4)/2</td>
</tr>
<tr>
<td></td>
<td>VVH1 – VVH</td>
<td>–0.25</td>
<td></td>
<td>0.1</td>
<td>V</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VVH4 – VVH</td>
<td>–0.25</td>
<td></td>
<td>0.1</td>
<td>V</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VVHH</td>
<td></td>
<td></td>
<td>0.5</td>
<td>V</td>
<td>2</td>
<td>High-level coupling</td>
</tr>
<tr>
<td></td>
<td>VVHL</td>
<td></td>
<td></td>
<td>0.5</td>
<td>V</td>
<td>2</td>
<td>High-level coupling</td>
</tr>
<tr>
<td></td>
<td>VVLL</td>
<td></td>
<td></td>
<td>0.5</td>
<td>V</td>
<td>2</td>
<td>Low-level coupling</td>
</tr>
<tr>
<td><strong>Vertical transfer clock voltage</strong></td>
<td>VVLH</td>
<td></td>
<td></td>
<td>0.5</td>
<td>V</td>
<td>2</td>
<td>Low-level coupling</td>
</tr>
<tr>
<td><strong>Horizontal transfer clock voltage</strong></td>
<td>V&lt;sub&gt;ϕ&lt;/sub&gt;H</td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>VHL</td>
<td>–0.05</td>
<td>0</td>
<td>0.05</td>
<td>V</td>
<td>3</td>
<td>Cross-point voltage</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;ϕ&lt;/sub&gt;R</td>
<td>V&lt;sub&gt;ϕ&lt;/sub&gt;H/2</td>
<td></td>
<td></td>
<td></td>
<td>3</td>
<td></td>
</tr>
<tr>
<td><strong>Reset gate clock voltage</strong></td>
<td>V&lt;sub&gt;ϕ&lt;/sub&gt;RG</td>
<td>3.4</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;RGLH&lt;/sub&gt; – V&lt;sub&gt;RGLL&lt;/sub&gt;</td>
<td>0.4</td>
<td></td>
<td></td>
<td>V</td>
<td>4</td>
<td>Low-level coupling</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;RGL&lt;/sub&gt; – V&lt;sub&gt;RGLm&lt;/sub&gt;</td>
<td>0.5</td>
<td></td>
<td></td>
<td>V</td>
<td>4</td>
<td>Low-level coupling</td>
</tr>
<tr>
<td><strong>Substrate clock voltage</strong></td>
<td>V&lt;sub&gt;ϕ&lt;/sub&gt;SUB</td>
<td>22.5</td>
<td>23.5</td>
<td>24.5</td>
<td>V</td>
<td>5</td>
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## Clock Equivalent Circuit Constants

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
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<tbody>
<tr>
<td>Capacitance between vertical transfer clock and GND</td>
<td>$C_{\phi V1A}$, $C_{\phi V1B}$</td>
<td>1200 pF</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
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<tr>
<td></td>
<td>$C_{\phi V2A}$, $C_{\phi V2B}$</td>
<td>2700 pF</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
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<td></td>
<td>$C_{\phi V3A}$, $C_{\phi V3B}$</td>
<td>680 pF</td>
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<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V4A}$, $C_{\phi V4B}$</td>
<td>1800 pF</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
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<tr>
<td></td>
<td>$C_{\phi st}$, $C_{\phi st Vhld}$</td>
<td>1 pF</td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
<td>Capacitance between vertical transfer clocks</td>
<td>$C_{\phi V1AV2A}$, $C_{\phi V1BV2B}$</td>
<td>220 pF</td>
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<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V1AV4B}$, $C_{\phi V1BV4A}$</td>
<td>47 pF</td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V2AV3A}$, $C_{\phi V2BV3B}$</td>
<td>220 pF</td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V3AV4A}$, $C_{\phi V3BV4B}$</td>
<td>390 pF</td>
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<td>pF</td>
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<tr>
<td></td>
<td>$C_{\phi V4BVst}$, $C_{\phi V4BVhld}$</td>
<td>47 pF</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$C_{\phi V3BVst}$, $C_{\phi V4BVhld}$</td>
<td>47 pF</td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
<td>Capacitance between horizontal transfer clock and GND</td>
<td>$C_{\phi H1}$</td>
<td>32 pF</td>
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<td>pF</td>
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<td></td>
<td>$C_{\phi H2}$</td>
<td>30 pF</td>
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<td></td>
<td>pF</td>
<td></td>
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<tr>
<td>Capacitance between horizontal transfer clocks</td>
<td>$C_{\phi HH}$</td>
<td>56 pF</td>
<td></td>
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<td>pF</td>
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<tr>
<td>Capacitance between reset gate clock and GND</td>
<td>$C_{\phi RG}$</td>
<td>1 pF</td>
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<td>pF</td>
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<tr>
<td>Capacitance between substrate clock and GND</td>
<td>$C_{\phi SUB}$</td>
<td>330 pF</td>
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<tr>
<td>Capacitance between horizontal final stage transfer clock and GND</td>
<td>$C_{\phi L1H}$</td>
<td>1 pF</td>
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<td>pF</td>
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<tr>
<td>Vertical transfer clock series resistance</td>
<td>$R_{\phi V1A}$, $R_{\phi V1B}$, $R_{\phi V4A}$, $R_{\phi V4B}$, $R_{\phi st}$, $R_{\phi st Vhld}$</td>
<td>39 Ω</td>
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<td>Ω</td>
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<tr>
<td></td>
<td>$R_{\phi V2A}$, $R_{\phi V2B}$, $R_{\phi V3A}$, $R_{\phi V3B}$</td>
<td>82 Ω</td>
<td></td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Vertical transfer clock ground resistance</td>
<td>$R_{GND}$</td>
<td>15 Ω</td>
<td></td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>Horizontal transfer clock series resistance</td>
<td>$R_{\phi H1A}$, $R_{\phi H1B}$</td>
<td>18 Ω</td>
<td></td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$R_{\phi H2A}$, $R_{\phi H2B}$</td>
<td>16 Ω</td>
<td></td>
<td></td>
<td>Ω</td>
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<tr>
<td>Substrate clock series resistance</td>
<td>$R_{\phi SUB}$</td>
<td>300 kΩ</td>
<td></td>
<td></td>
<td>kΩ</td>
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Vertical transfer clock equivalent circuit

Horizontal transfer clock equivalent circuit
Drive Clock Waveform Conditions

1. Readout clock waveform

\[ V_{\phi 1A}, V_{\phi 1B}, V_{\phi 3T} \]

\[ V_{\phi 2A}, V_{\phi 2B} \]

\[ V_{\phi 3A}, V_{\phi 3B} \]

\[ V_{\phi 4A}, V_{\phi 4B}, V_{\phi HLD} \]

\[ V_{VH} = (V_{VH2} + V_{VH3})/2 \]

\[ V_{VL} = (V_{VL1} + V_{VL4})/2 \]

\[ V_{\phi V} = V_{VH1} - V_{VHL n} \text{ (n = 1 to 4)} \]
3. Horizontal transfer clock waveform

VCR is the cross-point voltage of the horizontal transfer clocks $H_{\phi 1A}, H_{\phi 1B}, LH_{\phi 1}$ and $H_{\phi 2A}, H_{\phi 2B}$ waveforms that is on the $H_{\phi 1A}, H_{\phi 1B}, LH_{\phi 1}$ rise side.
“two” is the overlapped period with $t_{wh}$ and $twl$ of the horizontal transfer clocks $H_{\phi 1A}, H_{\phi 1B}, LH_{\phi 1}$ and $H_{\phi 2A}, H_{\phi 2B}$.

4. Reset gate clock waveform

VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.
$$VRGL = \frac{VRGLH + VRGLL}{2}$$
Assuming VRGH is the minimum value during the interval $t_{wh}$, then;
$$V_{\phi RG} = VRGH - VRGL$$
VRGLm is the negative overshoot level during the falling edge of RG.

5. Substrate clock waveform
Clock Switching Characteristics

(Horizontal drive frequency: 36.0MHz)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>twh</th>
<th>twl</th>
<th>tr</th>
<th>tf</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Readout clock</td>
<td>Vr</td>
<td>1.52</td>
<td>1.72</td>
<td>0.5</td>
<td>0.5</td>
<td>(\mu s)</td>
<td>During readout</td>
</tr>
<tr>
<td>Vertical transfer clock</td>
<td>V(\phi1A), V(\phi1B), V(\phi2A), V(\phi2B), V(\phi3A), V(\phi3B), V(\phi4A), V(\phi4B), V(\phiST), V(\phiHLD)</td>
<td>15</td>
<td>250</td>
<td>ns</td>
<td>When using CXD3400N</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Horizontal transfer clock</td>
<td>LH(\phi1), H(\phi1A), H(\phi1B)</td>
<td>8</td>
<td>9</td>
<td>5</td>
<td>6</td>
<td>ns</td>
<td>When driving at 3.6V during imaging, (t_f \geq t_r - 2ns)</td>
</tr>
<tr>
<td></td>
<td>H(\phi2A), H(\phi2B)</td>
<td>8</td>
<td>9</td>
<td>5</td>
<td>6</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Reset gate clock</td>
<td>(\phiRG)</td>
<td>4</td>
<td>5.5</td>
<td>17.2</td>
<td>2</td>
<td>3</td>
<td>ns</td>
</tr>
<tr>
<td>Substrate clock</td>
<td>(\phiSUB)</td>
<td>0.9</td>
<td>1.8</td>
<td>0.25</td>
<td>0.25</td>
<td>(\mu s)</td>
<td>When draining charge</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>two</th>
<th>Unit</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Horizontal transfer clock</td>
<td>LH(\phi1), H(\phi1A), H(\phi1B), H(\phi2A), H(\phi2B)</td>
<td>8</td>
<td>9</td>
<td>ns</td>
</tr>
</tbody>
</table>

Spectral Sensitivity Characteristics

(excludes lens characteristics and light source characteristics)
Image Sensor Characteristics (Center cut-out drive, 30 frame/s)

(Ta = 25°C)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
<th>Measurement method</th>
<th>Remarks</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sensitivity 1</td>
<td>S1</td>
<td>300</td>
<td>380</td>
<td></td>
<td>mV</td>
<td>1/30s accumulation</td>
<td></td>
</tr>
<tr>
<td>Sensitivity 2</td>
<td>S2</td>
<td>1000</td>
<td>1500</td>
<td></td>
<td>mV</td>
<td>1/30s accumulation</td>
<td></td>
</tr>
<tr>
<td>Saturation signal</td>
<td>Vsat</td>
<td>350</td>
<td></td>
<td></td>
<td>mV</td>
<td>Ta = 60°C</td>
<td></td>
</tr>
<tr>
<td>Smear</td>
<td>Sm</td>
<td>–104</td>
<td>–96</td>
<td></td>
<td>dB</td>
<td>4</td>
<td></td>
</tr>
<tr>
<td>Video signal shading</td>
<td>SH</td>
<td></td>
<td>20%</td>
<td></td>
<td>%</td>
<td>5</td>
<td>Zone 0 and I</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>25%</td>
<td></td>
<td>%</td>
<td>5</td>
<td>Zone 0 to II'</td>
</tr>
<tr>
<td>Dark signal</td>
<td>Vdt</td>
<td></td>
<td>2</td>
<td></td>
<td>mV</td>
<td>Ta = 60°C, 1/30s accumulation</td>
<td></td>
</tr>
<tr>
<td>Dark signal shading</td>
<td>△Vdt</td>
<td></td>
<td>1</td>
<td></td>
<td>mV</td>
<td>Ta = 60°C, 1/30s accumulation*¹</td>
<td></td>
</tr>
<tr>
<td>Lag</td>
<td>Lag</td>
<td></td>
<td>0.5</td>
<td></td>
<td>%</td>
<td>8</td>
<td></td>
</tr>
</tbody>
</table>

*¹ Excludes vertical dark signal shading caused by the vertical register high-speed transfer.

Zone Definition of Video Signal Shading

Measurement System

Note) Adjust the amplifier gain so that the gain between [ * A] and [ * B] equals 1.
Image Sensor Characteristics Measurement Method

Measurement conditions
1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.

2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black (OB) level is used as the reference for the signal output, and the value measured at point [*B] of the measurement system is used.

Definition of Standard Imaging Conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F8. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
This indicates the standard imaging condition I with the IR cut filter removed.

◆ Standard imaging condition III:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity 1
Set the measurement condition to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal output (Vs1) at the center of the screen, and substitute the value into the following formula.

\[ S1 = Vs1 \times (100/30) \text{ [mV]} \]

2. Sensitivity 2
Set the measurement condition to the standard imaging condition II. After setting the electronic shutter mode with a shutter speed of 1/500s, measure the signal output (Vs2) at the center of the screen, and substitute the value into the following formula.

\[ S2 = Vs2 \times (500/30) \text{ [mV]} \]

3. Saturation signal
Set the measurement condition to the standard imaging condition III. After adjusting the luminous intensity to 10 times the intensity with the average value of the signal output, 150mV, measure the minimum value of the signal output.

4. Smear
Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with the average value of the signal output, 150mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (VSm) of the signal output, and substitute the value into the following formula.

\[ Sm = 20 \times \log ((VSm/150) \times (1/500) \times (1/10)) \text{ [dB]} \text{ (1/10V method conversion value)} \]
5. Video signal shading
Set the measurement condition to the standard imaging condition III. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the signal output is 150mV. Then measure the maximum value (Vmax) and the minimum value (Vmin) of the signal output, and substitute the values into the following formula.

\[ SH = \frac{(V_{\text{max}} - V_{\text{min}})}{150} \times 100\% \]

6. Dark signal
Measure the average value (Vdt) of the signal output with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as the reference.

7. Dark signal shading
After the measurement item 6, measure the maximum value (Vd_{\text{max}}) and the minimum value (Vd_{\text{min}}) of the dark signal output, and substitute the values into the following formula.

\[ \Delta V_{\text{dt}} = V_{\text{dmax}} - V_{\text{dmin}} \text{ [mV]} \]

8. Lag
Adjust the signal output value generated by the strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal level (Vlag), and substitute the value into the following formula.

\[ \text{Lag} = \frac{(V_{\text{lag}}/150)}{100\%} \]
Drive Circuit

Connecting a 1MΩ grounding resistor to Pin 22 (φSUB) is not necessary. The value of the capacitor connected to Pin 22 (φSUB) is approximately 10μF.

Connecting a constant current source with low collector output capacitance (current value 2 to 6mA) to Pin 13 (VOUT).

When performing oscillation, connect a resistor and/or a capacitor to the base. Select the optimum value from approximately 2 to 6mA for the constant current value and the rear-end emitter current value in consideration of the load capacitance.

The vs value can be adjusted in the range of 0.0 to 5.0V ± 5%. Raising the vs potential reduces heat generated at the constant current source and buffer connected to the VOUT pin. Be careful because the value of the resistor connected to the constant current source and buffer transistor varies according to the value of vs.

(VOUTDC – Vs – 0.8) /3 [kΩ] When emitter current is 3mA.

(VOUTDC – Vs – 0.8) /4.5 [kΩ] When constant current is 4.5mA.

(VOUTDC – Vs – 0.8) /5 [kΩ] When constant current is 5mA.

(CxD3400N)

(Vb – Vs – 0.8) / (15 – Vb) /10 [kΩ]

(VOUTDC – Vs – 0.8) /3 [kΩ]

(VOUTDC – Vs – 0.8) /4.5 [kΩ]
Drive Timing Chart

All-pixel Scan Mode (15 frame/s)  Vertical Direction

TGVD
TGHD
V1
V2A
V3A
V4
V2B
V3B
VSTR
VHLD
CCD OUT
PBLK
CLPOB
CLPDM

*A* 1456 (0) 12

60

1456 (0)

SUB

"TGVD in this chart is noted at 1456H (1H: 1650clocks). (1clock = 36.0MHz)"

"C" 62

978H

1

2

3

965

966

"B" 104072

60H + θ (1376steps)

1038

High-speed sweep
All-pixel Scan Mode (12.5 frame/s)  Vertical Direction

TGVD
TGHD
V1
V2A
V2B
V3A
V4
V2B
V3B
VSTR
VHLD
CCD OUT
PBLK
CLPOB
CLPDM

1450 (0) 12

TGVD in this chart is noted at 1450H (1H: 1600clocks). (1clock = 29.0MHz)

High-speed sweep
52H + (1388steps)
All-pixel Scan Mode (22.5 frame/s)  Vertical Direction

TGVD
TGHD
V1
V2A
V3A
V4
V2B
V3B
VSTR
VHLD
CCD OUT
PBLK
CLPOB
CLPDM

10H \( \text{H} \)

TGVD in this chart is noted at 10H \( \text{H} \) (1H: 1600 clocks). (1 clock = 36.0 MHz)
Center Cut-out Mode (30 frames) Vertical Direction

TGVD
TGHD
SUB
V1
V2A
V2B
V3A
V4B
V4
V3B
VSTR
VHL.D
CCD OUT
PBLK
CLPOB
CLPDM

Fractional adjustment line

* TGVD in this chart is noted at 750H (1H: 1598 clocks) + 1H (2700 clocks: fractional adjustment line). (1 clock = 36.0 MHz)
All-pixel Scan Mode (15 frame/s)
Horizontal Direction - High-speed Sweep Block

1650 (0) All-pixel scan mode (15 frame/s)
1600 (0) All-pixel scan mode (12.5 frame/s)

Drive frequency: 36.0MHz (15 frame/s)
29.0MHz (12.5 frame/s)

* Synchronize the rising edge of SUB with the first falling edge of VSTR (a) counting from the falling edge of TGHD,
and synchronize the falling edge of SUB with the first rising edge of VHLD (b) counting from (a).

* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
The numbers on the upper level are for 36.0MHz, and the numbers in parentheses on the lower level are for 29.0MHz.
Center Cut-out Mode (30 frame/s, 25 frame/s)

Horizontal Direction High-speed Sweep Block [A]

Drive frequency: 36.0MHz (30 frame/s)
29.0MHz (25 frame/s)

- Synchronize the rising edge of SUB with the first falling edge of VSTR (a) counting from the falling edge of TGHD, and synchronize the falling edge of SUB with the first rising edge of VHLD (b) counting from (a).

The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.

The numbers on the upper level are for 36.0MHz, and the numbers in parentheses on the lower level are for 29.0MHz.
All-pixel Scan Mode (15 frame/s, 22.5 frame/s)
1650 (0) All-pixel scan mode (15 frame/s)
1600 (0) All-pixel scan mode (12.5 frame/s)
1598 (0) All-pixel scan mode (22.5 frame/s)
1556 (0) Center cut-out mode (30 frame/s)
1600 (0) Center cut-out mode (25 frame/s)

Drive frequency: 36.0MHz (15 frame/s, 30 frame/s, 22.5 frame/s)
29.0MHz (12.5 frame/s, 25 frame/s)

* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
The numbers on the upper level are for 36.0MHz, and the numbers in parentheses on the lower level are for 29.0MHz.
When there is no number in parentheses, the count is the same for both 36.0MHz and 29.0MHz.
All-pixel Scan Mode (15 frame/s, 12.5 frame/s, 22.5 frame/s)
Center Cut-out Mode (30 frame/s, 25 frame/s)

Horizontal Direction Readout Block [C]

Drive frequency: 36.0MHz (15 frame/s, 30 frame/s, 22.5 frame/s)
29.0MHz (12.5 frame/s, 25 frame/s)

* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD. The numbers on the upper level are for 36.0MHz, and the numbers in parentheses on the lower level are for 29.0MHz.
Center Cut-out Mode (30 frame/s, 25 frame/s)

Horizontal Direction Frame Shift Block [D]

Drive frequency: 36.0MHz (30 frame/s)
29.0MHz (25 frame/s)

- 25 -

1598 (0) Center cut-out mode (30 frame/s)
1556 (0) Center cut-out mode (25 frame/s)

V1
V2A/V2B
V3A/V3B
V4
V5TR
VHLD

#129 Center cut-out mode (30 frame/s): from the falling edge of 21H TGHD to 1050th clock (end)
#130 Center cut-out mode (25 frame/s): from the falling edge of 17H TGHD to 92nd clock (end)

* SUB pulse generation is prohibited during the frame shift period.

* The numbers at the output pulse transition points indicate the count at the rising edge of the clock from the falling edge of TGHD.
The numbers on the upper level are for 36.0MHz, and the numbers in parentheses on the lower level are for 29.0MHz.
Notes On Handling

1. Static charge prevention
   Image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material. Also use conductive shoes.
   (2) Use a wrist strap when handling directly.
   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling image sensors.
   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Soldering
   (1) Make sure the temperature of the upper surface of the seal glass resin adhesive portion of the package does not exceed 80°C.
   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in 2 seconds or less. For repairs and remount, cool sufficiently.
   (3) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3. Protection from dust and dirt
   Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.
   (1) Perform all lens assembly and other work in a clean room (class 1000 or less).
   (2) Do not touch the glass surface with hand and make any object contact with it. If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity, ionized air is recommended.)
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

4. Installing (attaching)
   (1) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)

   ![Plastic package and Cover glass](image)

   **Compressive strength**
   - 50N
   - 50N
   - 1.2Nm

   (2) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
   (3) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
(4) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

(5) If the lead bend repeatedly and the metal, etc., clash or rub against the package, dust may be generated by the fragments of resin.

(6) Acrylate anaerobic adhesives are generally used to attach image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives to hold the image sensor in place until the adhesive completely hardens. (reference)

5. Others

(1) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminance objects are imaged with the exposure level controlled by the electronic iris, the luminance of the image-plane may become excessive and discoloration of the color filters may be accelerated. In such a case, arrangements such as using an automatic iris with the imaging lens or automatically closing the shutter during power-off are advisable. For continuous use under harsh conditions exceeding the normal conditions of use, consult your Sony representative.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) Brown stains may be seen on the bottom or side of the package. But this does not affect the characteristics.

(4) This image sensor has sensitivity in the near infrared area. Its focus may not match in the same condition under visible light/near infrared light because of aberration. Incident light component of long wavelength which transmits the silicon substrate may have bad influence upon image.
1. "A" is the center of the effective image area.
2. The two points "B" of the package are the horizontal reference. The point "B'" of the package is the vertical reference.
3. The bottom "C" of the package, and the top of the cover glass "D" are the height reference.
4. The center of the effective image area relative to "B" and "B'" is (H, V) = (8.0, 7.1) ± 0.075mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°
6. The height from the bottom "C" to the effective image area is 1.41mm ± 0.1mm. The height from the top of the cover glass "D" to the effective image area is 1.49mm ± 0.15mm
7. The tilt of the effective image area relative to the bottom "C" is less than 35µm. The tilt of the effective image area relative to the top "D" of the cover glass is less than 50µm.
8. The thickness of the cover glass is 0.5mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.

PACKAGE STRUCTURE

<table>
<thead>
<tr>
<th>PACKAGE MATERIAL</th>
<th>Plastic</th>
</tr>
</thead>
<tbody>
<tr>
<td>LEAD TREATMENT</td>
<td>GOLD PLATING</td>
</tr>
<tr>
<td>LEAD MATERIAL</td>
<td>42 ALLOY</td>
</tr>
<tr>
<td>PACKAGE MASS</td>
<td>1.20g</td>
</tr>
<tr>
<td>DRAWING NUMBER</td>
<td>AS-A16(E)</td>
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