



1/3-Inch SOC Megapixel CMOS Digital Image Sensor

MT9M131I99STC (Pb-Free iCSP)
MT9M131C12STC (Pb-Free CLCC)

Features

- DigitalClarity[®] CMOS imaging technology
- System-on-a-Chip (SOC)—Completely integrated camera system
- Ultra-low power, high fidelity, progressive scan CMOS image sensor
- Superior low-light performance
- On-chip image flow processor (IFP) performs sophisticated processing:
 - Color recovery and correction
 - Sharpening, gamma, lens shading correction
 - On-the-fly defect correction
- Electronic pan, tilt, and zoom
- Automatic features:
 - Auto exposure, auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, auto defect identification and correction
 - Fully automatic Xenon and LED-type flash support
- Fast exposure adaptation
- Multiple parameter contexts
- Easy and fast mode switching
- Camera control sequencer automates:
 - Snapshots
 - Snapshots with flash
 - Video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats
- Output FIFO and integer clock divider:
 - Uniform pixel clocking

Applications

- Security
- Biometrics
- Videoconferencing
- Toys

Table 1: Key Performance Parameters

Parameter		Typical Value
Optical format		1/3-inch (5:4)
Active imager size		4.6mm (H) x 3.7mm (V), 5.9mm diagonal
Active pixels		1,280H x 1,024V
Pixel size		3.6 μ m x 3.6 μ m
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/ Maximum master clock		27 MPS/54 MHz
Frame Rate	SXGA (1,280 x 1,024)	15 fps at 54 MHz
	QSXGA (640 x 512)	30 fps at 54 MHz
Max. resolution at 60 fps w/ 54 MHz clock		640 x 512
ADC resolution		10-bit, dual on-chip
Responsivity		1.0 V/lux-sec (550nm)
Dynamic range		71dB
SNR _{MAX}		44dB
Supply voltage	I/O digital	1.8–3.1V
	Core digital	2.5–3.1V
	Analog	2.5–3.1V
Power consumption		170mW SXGA at 15 fps (54 MHz CLKIN) 90mW QSXGA at 30 fps (54 MHz low-power mode)
Operating temperature		–30 °C to +70 °C
Packaging		44-ball iCSP 48-pin CLCC

Table 2: Ordering Information

Part Number	Description
MT9M131I99STC	44-ball iCSP
MT9M131C12STC ES	48-pin CLCC ES
MT9M131C12STCD ES	Demo kit
MT9M131C12STCH ES	Demo kit headboard



MT9M131: SOC Megapixel Digital Image Sensor General Description

General Description

The Micron® Imaging MT9M131 is an SXGA-format single-chip camera with a 1/3-inch CMOS active-pixel digital image sensor. This device combines the MT9M011 image sensor core with fourth-generation digital image flow processor technology from Micron Imaging. It captures high-quality color images at SXGA resolution.

The MT9M131 features DigitalClarity™, Micron's breakthrough, low-noise CMOS imaging technology that achieves CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution designed specifically to meet the low-power, high fidelity demands of products such as security, biometrics, and video-conferencing cameras. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9M131 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure, automatic 50Hz/60Hz flicker avoidance, lens shading correction, auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both Xenon and LED-type flash light sources in several snapshot modes.

The MT9M131 can be programmed to output progressive-scan images up to 30 frames per second (fps) in preview power-saving mode, and 15 fps in full-resolution (SXGA) mode. In either mode, the image data can be output in any one of six 8-bit formats:

- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FRAME_VALID (FV) and LINE_VALID (LV) signals are output on dedicated signals, along with a pixel clock that is synchronous with valid data.

Table 3 lists typical values of MT9M131 performance parameters.

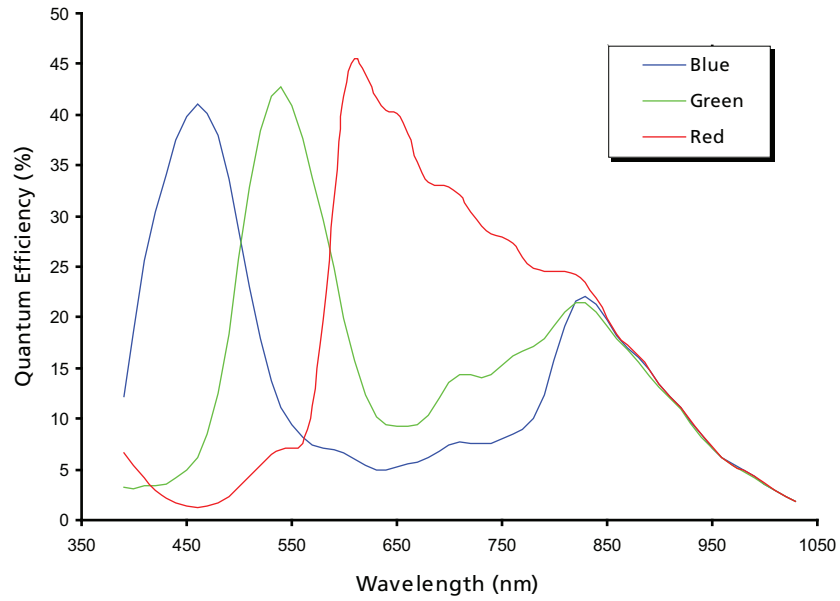
Table 3: MT9M131 Detailed Performance Parameters

Parameter	Typical
Output Gain	25 e-/LSB
Read Noise	7 e-RMS@ 16X



MT9M131: SOC Megapixel Digital Image Sensor General Description

Figure 1: MT9M131 Quantum Efficiency vs. Wavelength



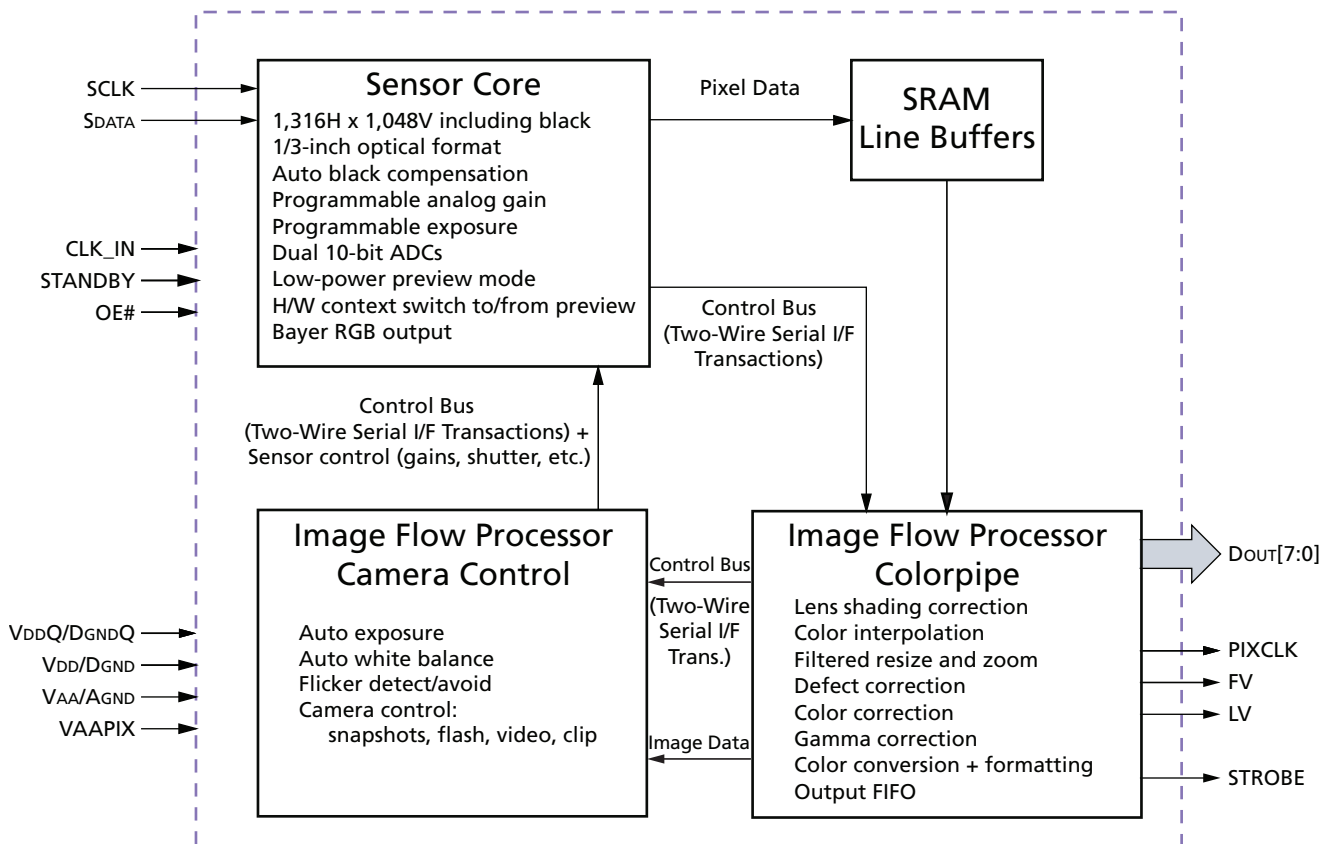


MT9M131: SOC Megapixel Digital Image Sensor Functional Overview

Functional Overview

The MT9M131 is a fully-automatic, single-chip camera, requiring only a power supply, lens, and clock source for basic operation. Output video is streamed through a parallel 8-bit DOUT port, shown in Figure 2.

Figure 2: Functional Block Diagram



The output pixel clock is used to latch data, while FV and LV signals indicate the active video. The MT9M131 internal registers are configured using a two-wire serial interface.

The device can be put in low-power sleep mode by asserting STANDBY and shutting down the clock. Output pins can be tri-stated by de-asserting OE#. Both tri-stating output pins and entry in standby mode also can be achieved by two-wire serial interface register writes.

The MT9M131 accepts input clocks up to 54 MHz, delivering up to 15 fps for SXGA resolution images, and up to 30 fps for QSXGA (full field-of-view, sensor pixel skipping) images. The device also supports a low-power preview configuration that delivers SXGA images at 7.5 fps and QSXGA images at 30 fps. The device can be programmed to slow the frame rate in low-light conditions to achieve longer exposures and better image quality.



MT9M131: SOC Megapixel Digital Image Sensor Typical Connection

Internal Architecture

Internally, the MT9M131 consists of a sensor core and an IFP. The IFP is divided in two sections: the colorpipe (CP), and the camera controller (CC). The sensor core captures raw Bayer-encoded images that are then input in the IFP. The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance, and to support snapshot modes.

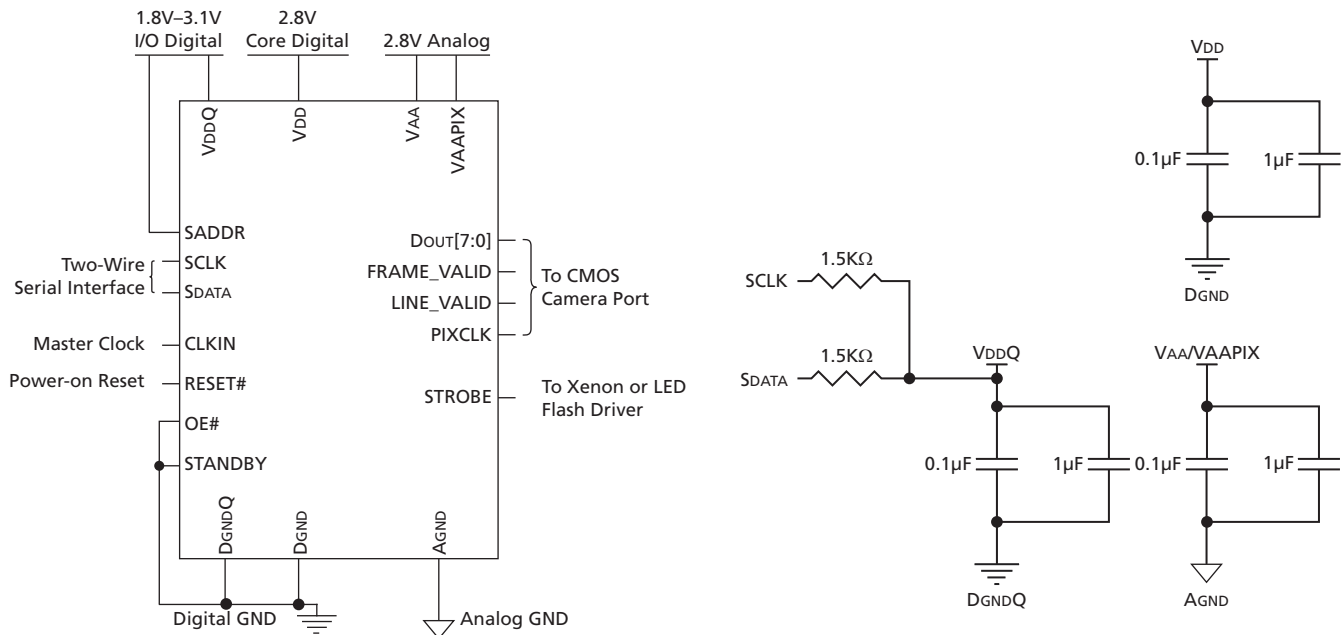
The MT9M131 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

- Standard FV/LV video interface with gated pixel clocks
- Standard video interface with uniform clocking
- Progressive ITU-R BT.656 marker-embedded video interface with either gated or uniform pixel clocking

Typical Connection

Figure 3 shows typical MT9M131 device connections.

Figure 3: Typical Configuration (Connection)



- Notes:
1. For two-wire serial interface, a 1.5KΩ resistor is recommended, but may be greater for slower two-wire speed.
 2. VDD, VAA, VAAPIX must all be at the same potential, though if connected, care must be taken to avoid excessive noise injection in the VAA/VAAPIX power domains.
 3. Logic levels of all input pins, that is, SADDR, CLKIN, SCLK, SDATA, OE#, STANDBY, and RESET# must be equal to VDDQ.



MT9M131: SOC Megapixel Digital Image Sensor Typical Connection

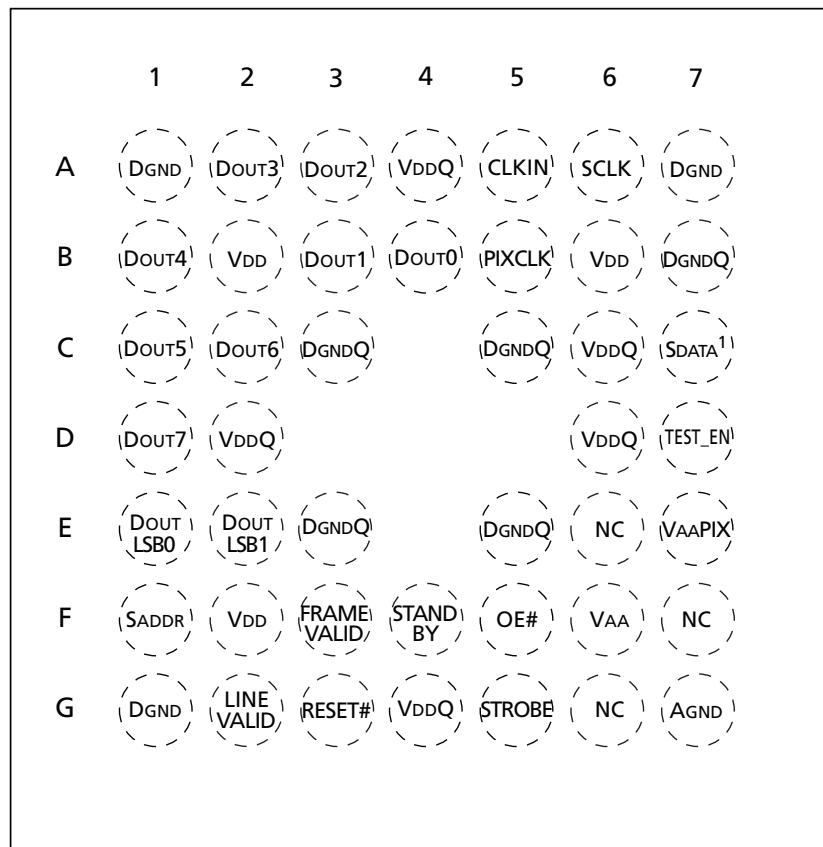
For low-noise operation, the MT9M131 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using ceramic capacitors. The use of inductance filters is not recommended.

The MT9M131 also supports different digital core (VDD/DGND) and I/O power (VDDQ/DGNDQ) power domains that can be at different voltages.

Pin/Ball Assignment

The MT9M131 is available in two configurations, iCSP and CLCC, illustrated in Figure 4 and Figure 5, respectively.

Figure 4: 44-Ball iCSP Assignment



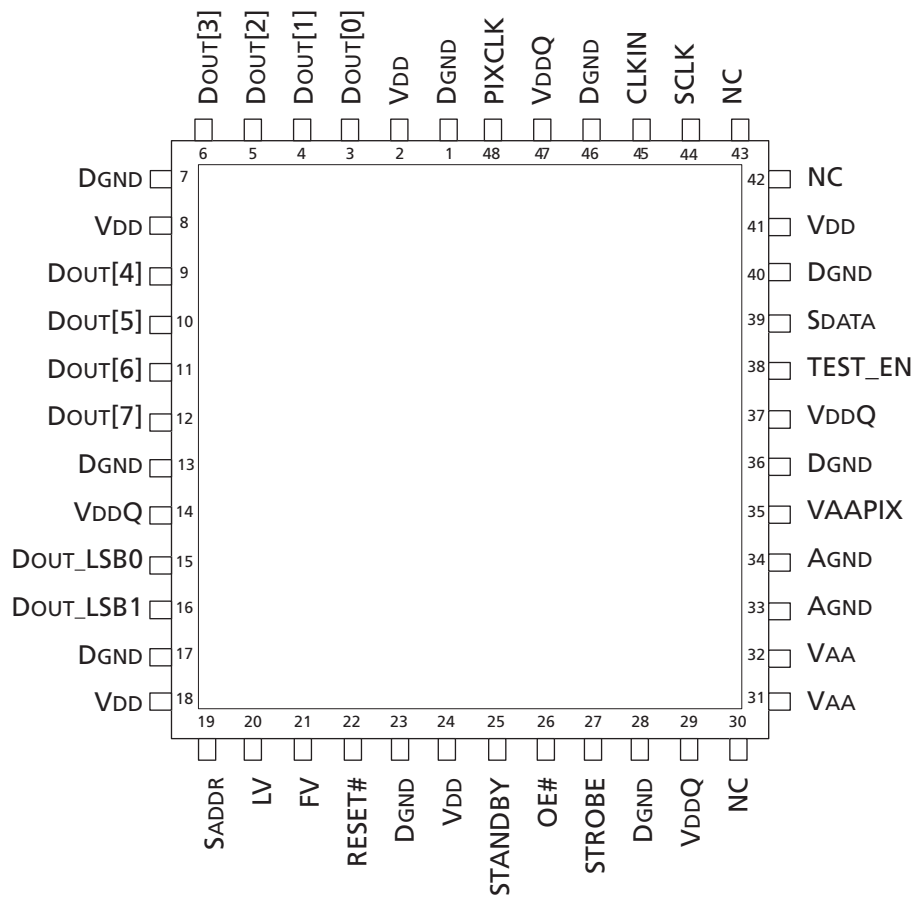
Top View
(Ball Down)

Notes: 1. The SDATA pin (ball C7) is bidirectional.



MT9M131: SOC Megapixel Digital Image Sensor Typical Connection

Figure 5: 48-Pin CLCC Assignment





MT9M131: SOC Megapixel Digital Image Sensor Typical Connection

Table 4: Pin/Ball Descriptions

Signal	iCSP Ball	CLCC Pin	Type	Default Operation	Description
CLKIN	A5	45	I/O	Input	Master clock in sensor
OE#	F5	26	I/O	Input	Active LOW: output enable for Data[7:0]
RESET#	G3	22	I/O	Input	Active LOW: asynchronous reset
SADDR	F1	19	I/O	Input	Two-wire serial interface DeviceID selection 1:0xBA, 0:0x90
SCLK	A6	44	I/O	Input	Two-wire serial interface clock
STANDBY	F4	45	I/O	Input	Active HIGH: disables imager
SDATA	C7	39	I/O	Input	Two-wire serial interface data I/O
TEST_EN	D7	38	I/O	Input	Tie to DGND for normal operation (Manufacturing use only)
DOUT0	B4	3	I/O	Output	Data output 2
DOUT1	B3	4	I/O	Output	Data output 3
DOUT2	A3	5	I/O	Output	Data output 4
DOUT3	A2	6	I/O	Output	Data output 5
DOUT4	B1	9	I/O	Output	Data output 6
DOUT5	C1	10	I/O	Output	Data output 7
DOUT6	C2	11	I/O	Output	Data output 8
DOUT7	D1	12	I/O	Output	Data output 9
DOUT_LSB0	E1	15	I/O	Output	Sensor bypass mode output 0—typically left unconnected for normal SOC operation
DOUT_LSB1	E2	16	I/O	Output	Sensor bypass mode output 1—typically left unconnected for normal SOC operation
FV	F3	21	I/O	Output	Active HIGH: FRAME_VALID; indicates active frame
LV	G2	20	I/O	Output	Active HIGH: LINE_VALID, DATA_VALID; indicates active pixel
PIXCLK	B5	48	I/O	Output	Pixel clock output
STROBE	G5	27	I/O	Output	Active HIGH: strobe (Xenon) or turn on (LED) flash
AGND	G7	33, 34		Supply	Analog ground
DGND	A1, A7, G1	1, 16, 13, 17, 23, 28, 36, 40, 46		Supply	Core digital ground
DGNDQ	B7, C3, C5, E3, Ee5			Supply	I/O digital ground
VAA	F6	31, 32		Supply	Analog power (2.5–3.1V)
VAAPIX	E7	35		Supply	Pixel array analog power supply (2.5–3.1V)
VDD	B2, B6, F2	2, 8, 18, 24, 41		Supply	Core digital power (2.5–3.1V)
VDDQ	A4, C6, D2, D6, G4	14, 29, 37, 47		Supply	I/O digital power (1.8–3.1V)
NC	E6, F7, G6	30, 42, 43		–	No connect

Note: All inputs and outputs are implemented with bidirectional buffers. Care must be taken that all inputs are driven and all outputs are driven if tri-stated.

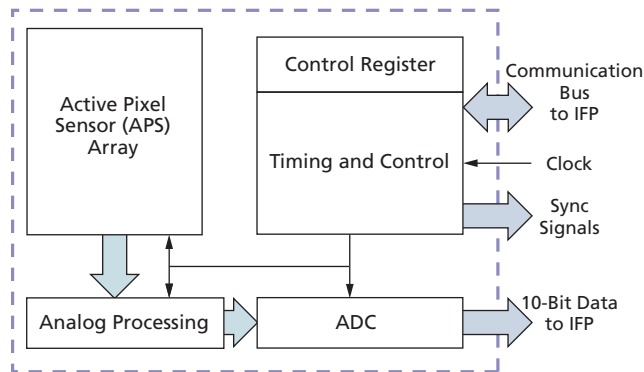


MT9M131: SOC Megapixel Digital Image Sensor Sensor Core Overview

Sensor Core Overview

The sensor consists of a pixel array of 1316 x 1048 total, an analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

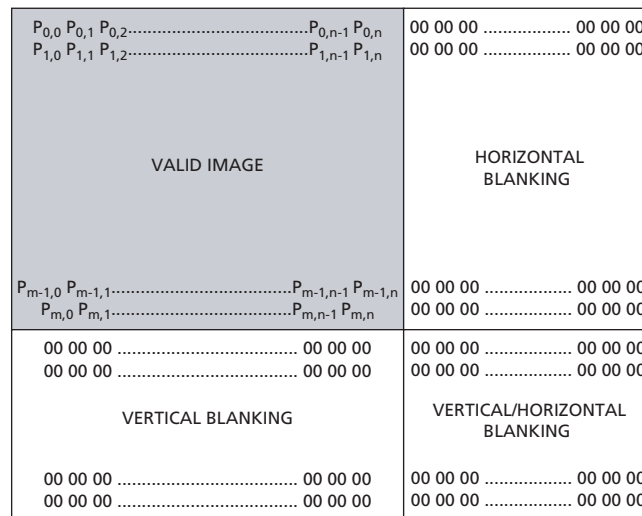
Figure 6: Sensor Core Block Diagram



Output Data Format

The MT9M131 sensor core image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, shown in Figure 7. LV is HIGH during the shaded region of the figure.

Figure 7: Spatial Illustration of Image Readout





MT9M131: SOC Megapixel Digital Image Sensor Electrical Specifications

Electrical Specifications

Table 5: Electrical Characteristics and Operating Conditions

T_A = Ambient = 25°C

Parameter	Condition	Min	Typ	Max	Unit
I/O digital voltage (VDDQ)		1.8		3.1	V
Core digital voltage (VDD)		2.5	2.8	3.1	V
Analog voltage (VAA)		2.5	2.8	3.1	V
Pixel supply voltage (VAAPIX)		2.5	2.8	3.1	V
Leakage current	STANDBY, no clocks			10	μA
Operating temperature	Measured at junction	-30		+70	°C

Note: VDD, VAA, and VAAPIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.

Table 6: I/O Parameters

Signal	Parameter	Definition	Condition	Min	Typ	Max	Unit
All outputs		Load capacitance				30	pF
		Output pin slew	2.8V, 30pF load		0.72		V/ns
			2.8V, 5pF load		1.25		V/ns
			1.8V, 30pF load		0.34		V/ns
	1.8V, 5pF load			0.51		V/ns	
	VOH	Output high voltage		VDDQ - 0.3		VDDQ	V
	VOL	Output low voltage		0		0.3	V
	IOH	Output high current	VDDQ = 2.8V, VOH = 2.4V	16		26.5	mA
			VDDQ = 1.8V, VOH = 1.4V	8		15	mA
	IOL	Output low current	VDDQ = 2.8V, VOL = 0.4V	15.9		21.3	mA
VDDQ = 1.8V, VOL = 0.4V			10.1		16.2	mA	
IOZ	Tri-state output leakage current				10	μA	
All inputs	VIH	Input high voltage	VDDQ = 2.8V	2.0			V
			VDDQ = 1.8V	1.2			V
	VIL	Input low voltage	VDDQ = 2.8V			0.9	V
			VDDQ = 1.8V			0.6	V
IIN	Input leakage current		-5		+5	μA	
PIN CAP	Ball input capacitance			3.5		pF	
CLKIN	Freq	Master clock frequency	Absolute minimum	2			MHz
			SXGA @ 15 fps	48		54	MHz



MT9M131: SOC Megapixel Digital Image Sensor Electrical Specifications

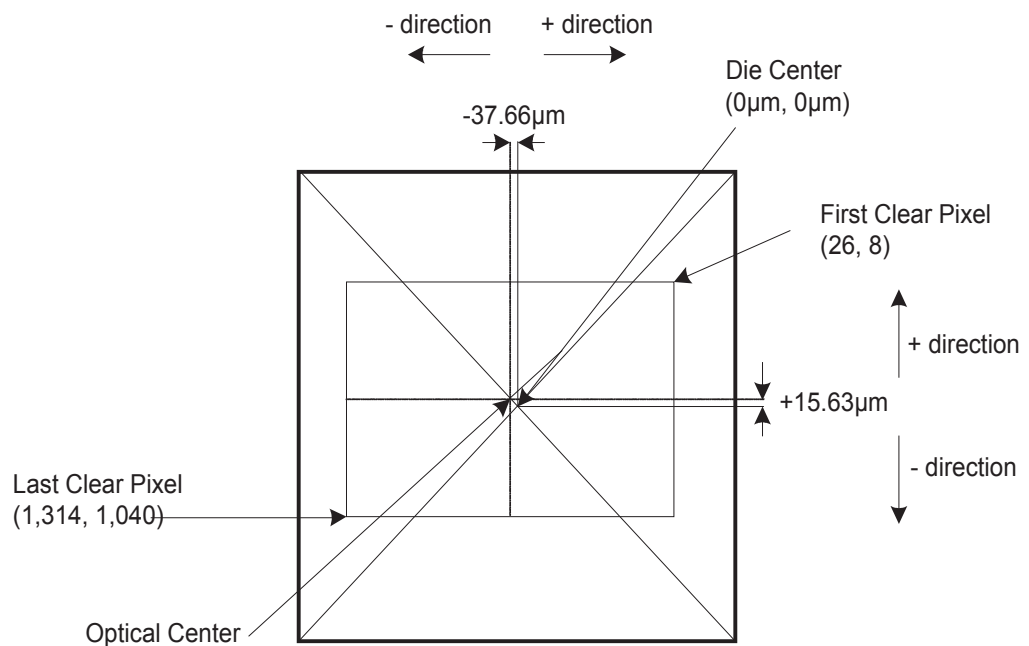
Caution Stresses above those listed in Table 7 may cause permanent damage to the device.

Table 7: Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
		Min	Max	
V _{SUPPLY}	Power supply voltage (all supplies)	-0.3	4.0	V
I _{SUPPLY}	Total power supply current	150		mA
I _{GND}	Total ground current	150		mA
V _{IN}	DC input voltage	-0.3	V _{DDQ} + 0.3	V
V _{OUT}	DC output voltage	-0.3	V _{DDQ} + 0.3	V
T _{STG}	Storage temperature	-40	85	°C

Notes: 1. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 8: Optical Center Diagram



Note: Figure not to scale.

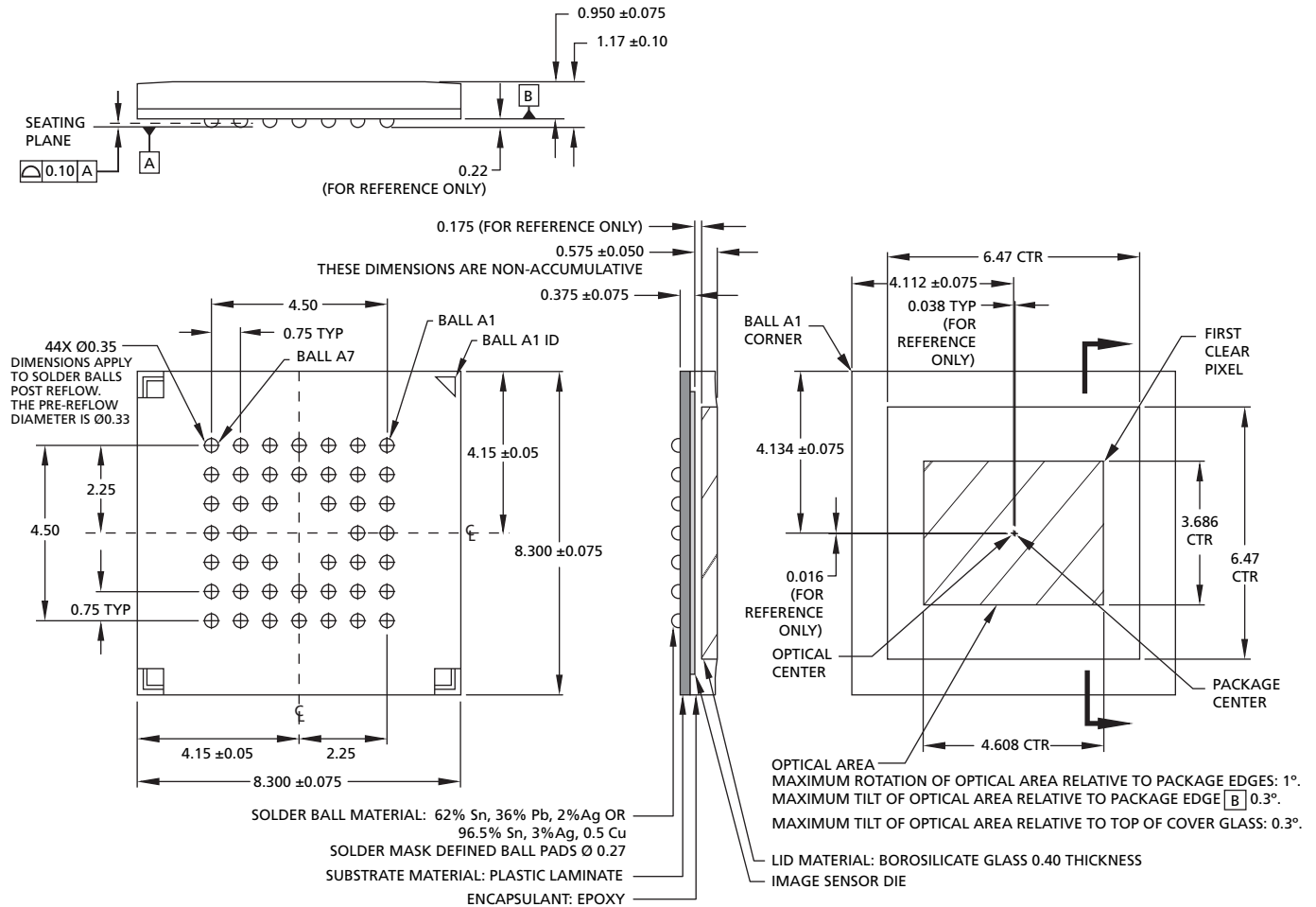


MT9M131: SOC Megapixel Digital Image Sensor Package Dimensions

Package Dimensions

The MT9M131 comes in two packages: the 44-ball iCSP package, shown in Figure 9, and the 48-pin CLCC package, shown in Figure 10 on page 13.

Figure 9: 44-Ball iCSP Package

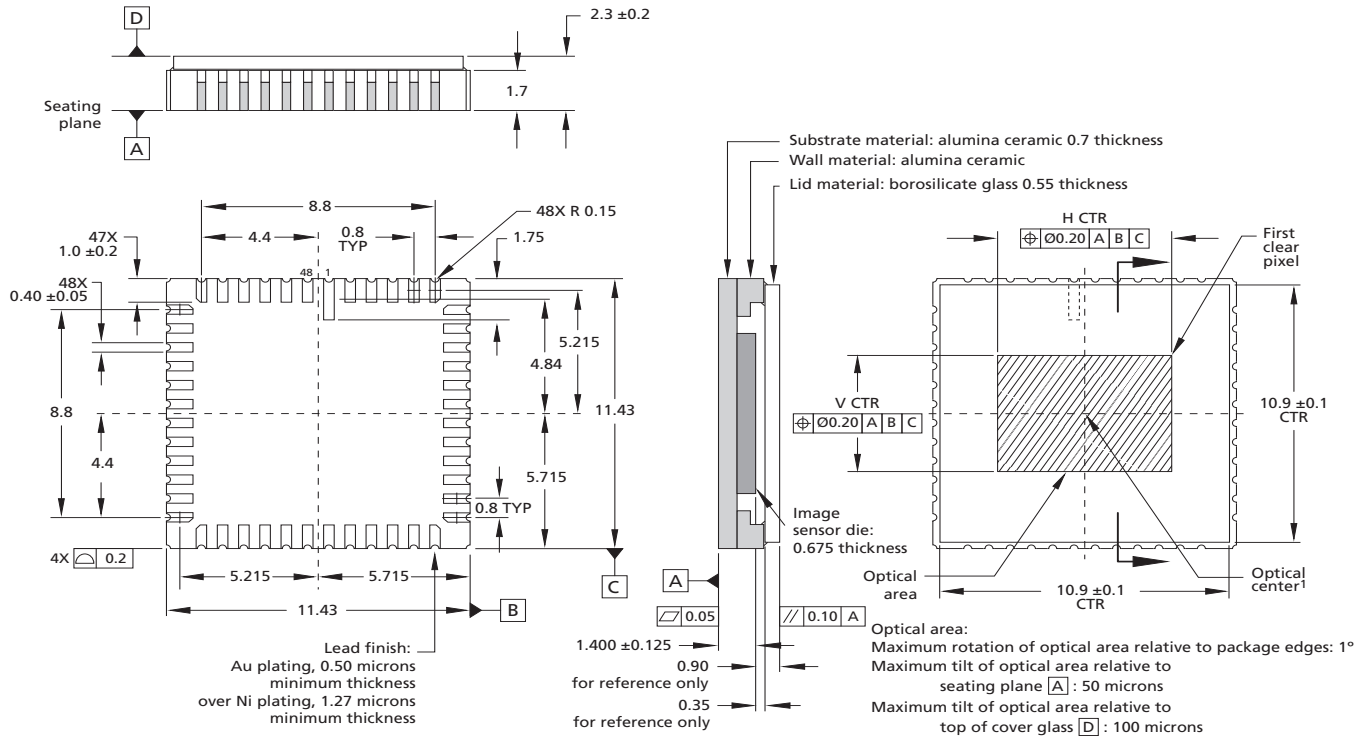


- Notes: 1. An IR-cut filter is required to obtain optimal image quality.
2. All dimensions are in millimeters.



MT9M131: SOC Megapixel Digital Image Sensor Package Dimensions

Figure 10: 48-Pin CLCC Package



8000 S. Federal Way, P.O. Box 6, Boise, ID 83707-0006, Tel: 208-368-3900

prodmktg@micron.com www.micron.com Customer Comment Line: 800-932-4992

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Preliminary: This data sheet contains initial characterization limits that are subject to change upon full characterization of production devices.



MT9M131: SOC Megapixel Digital Image Sensor Revision History

Revision History

Rev. A	3/16/2007
<ul style="list-style-type: none">• Initial release	